Xilinx Vivado based FPGA design and Zynq architecture

Course Overview

Day 1:

- 7-Series Architecture Overview
- **Lab 1: Vivado Design Flow**
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bitstream and verify in hardware.
- Zynq-7000 Architecture
- **Lab 2: Synthesizing a RTL Design**
  - Synthesize a design with the default settings as well as other settings changed and observe the effect.
- Implementation and Static Timing Analysis
- **Lab 3: Implementing the Design**
  - Implement the synthesized design of previous lab, perform timing analysis, generate bitstream, download the bitstream and verify the functionality.

Day 2:

- IP Integrator
- **Lab 4: Using the IP Catalog and IP Integrator**
  - Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design.
- Xilinx Design Constraints
- Using Vivado HLS
- **Lab 5: Creating Project and Understanding Reports**
  - Experience a basic design flow of Vivado HLS and review generated output.
- Improving Performance
- **Lab 6: Hardware Debugging**
  - Use Mark Debug feature and also available Integrated Logic Analyzer(ILA) core (available in IP Catalog) to debug the hardware.

Skills Gained

After completing this workshop, you will be able to:

- Describe the general Artix-7 All Programmable FPGA architecture
- Understand the Vivado design flow
- Create and debug HDL designs
- Configure FPGA and verify hardware operation
- Configure FPGA architecture features, such as Clock Manager, using the Architecture Wizard
- Communicate design timing objectives through the use of Xilinx Design Constraints

- Pinpoint design bottlenecks using the reports
- Utilize synthesis options to improve performance
- Create and integrate IP cores into design flow using IP Catalog
- Use Logic Analyzer to perform on-chip verification
- Perform simulation verifcation