MultilevelTopologies for IM drive with minimum DC power supplies

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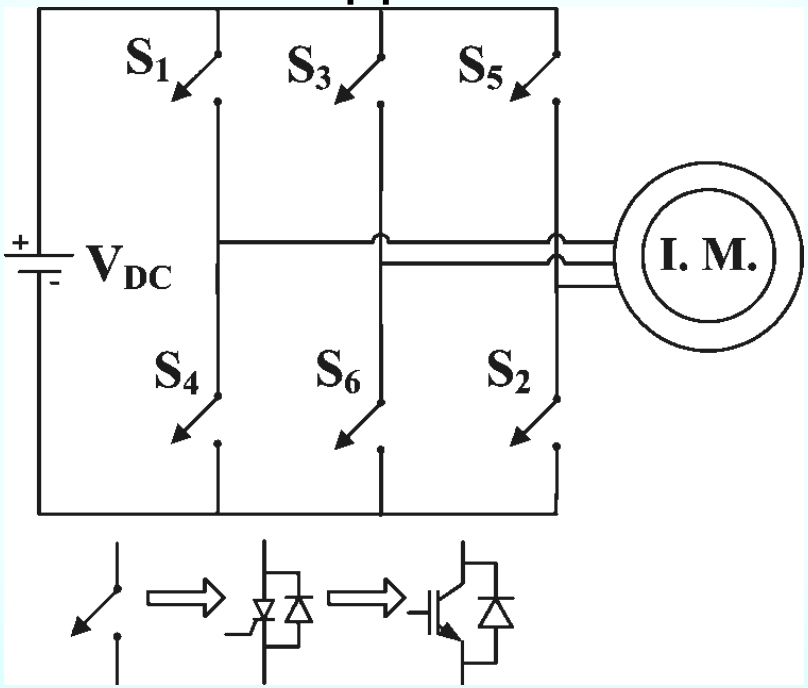
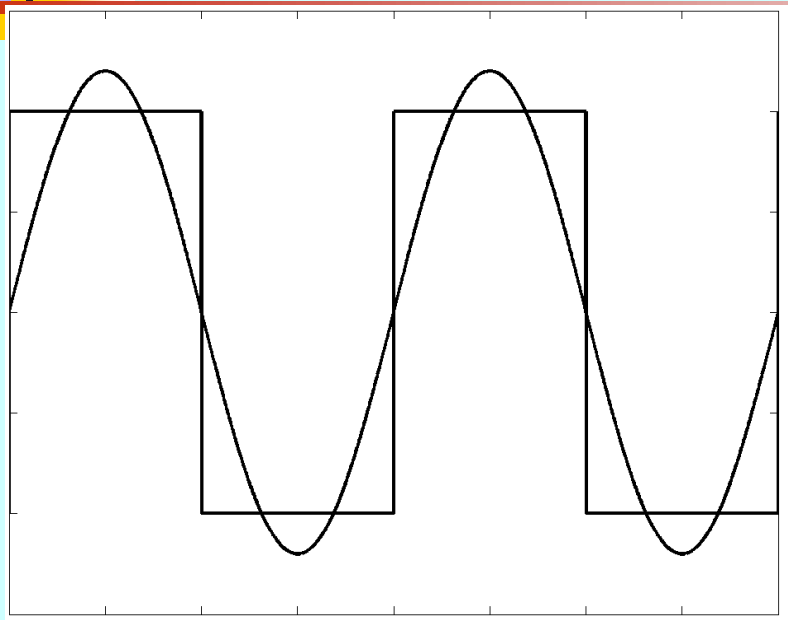
- Voltage source inverters (which convert DC power to AC power) have been receiving increasing attention in the past few years for high power and medium power induction motor drive applications

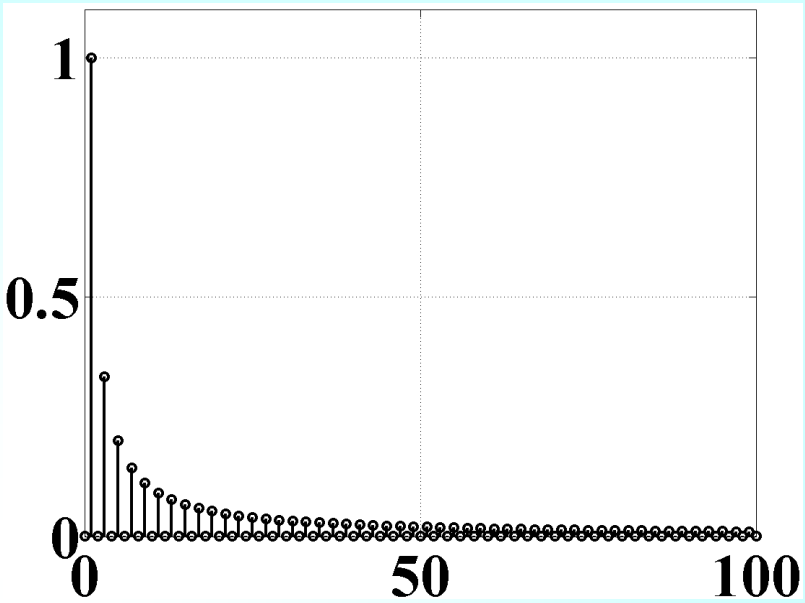


Conventional two-level inverter

Square Wave operation



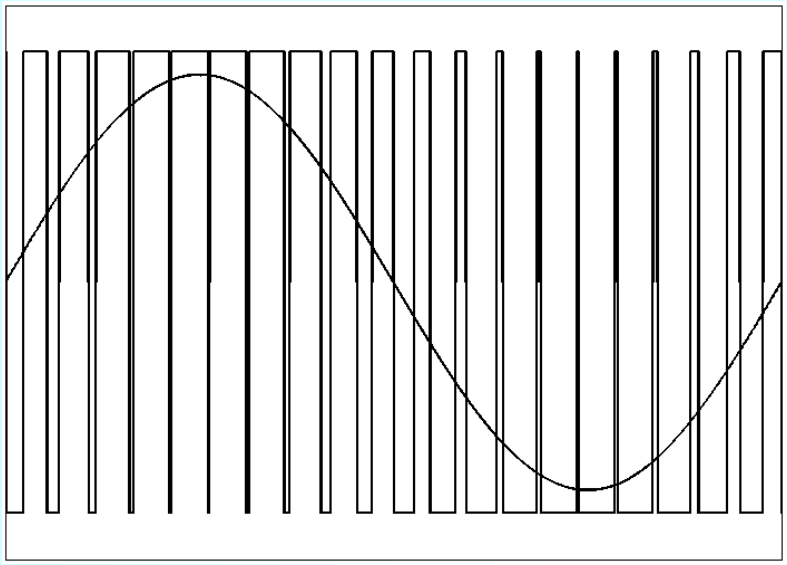
Inverter pole voltage in square wave operation



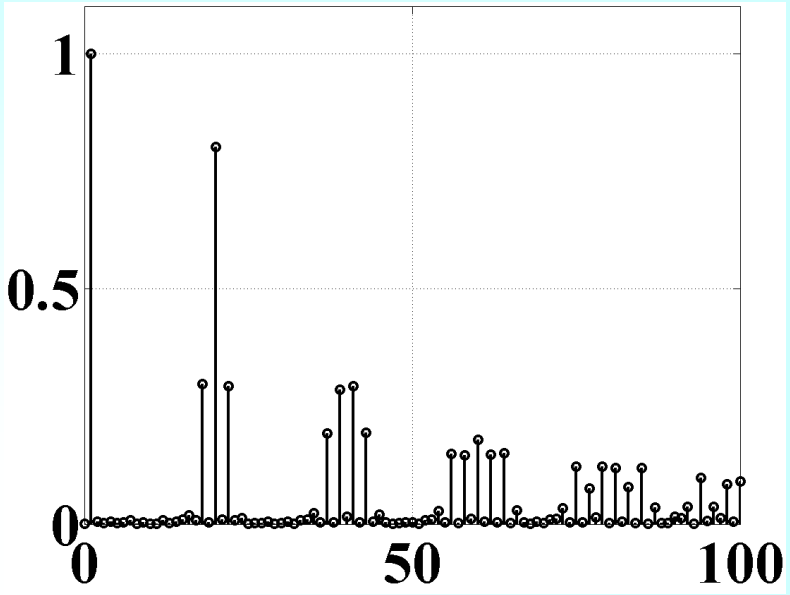
Normalized harmonics spectrum of pole voltage

- The pole voltage is rich in harmonics, which will reduce the efficiency of the overall system

Sine-Triangle PWM



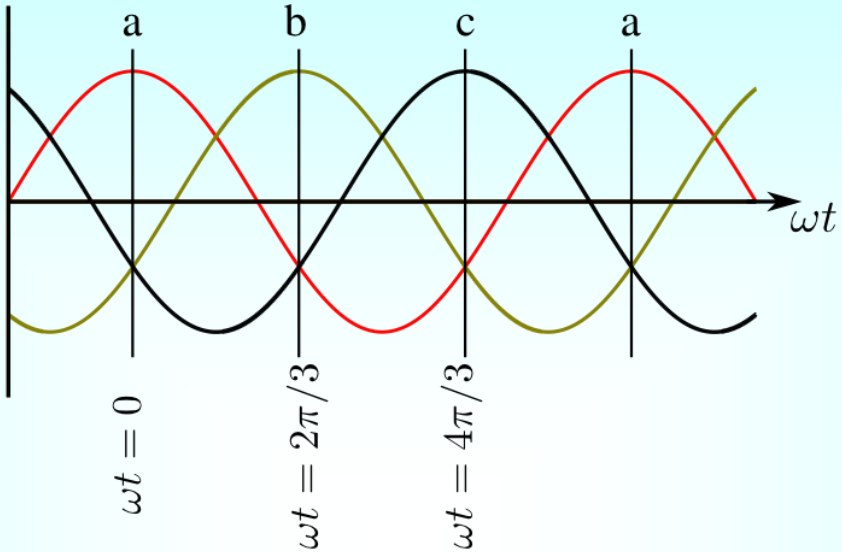
Inverter pole voltage
(sine-triangle PWM)

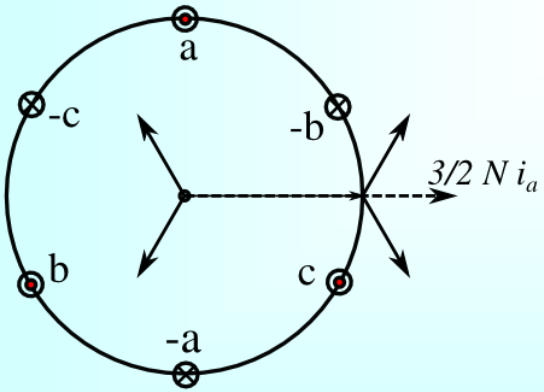


Normalized harmonics
spectrum of pole voltage

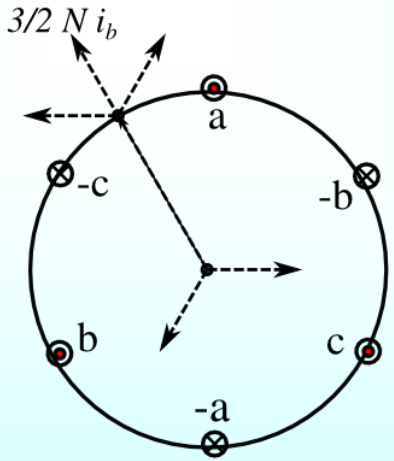
- The inverter output voltage and frequency are controlled
- The harmonic components in the inverter pole voltage are transferred to higher (switching) frequencies

Rotating air gap mmf with sinusoidal excitation

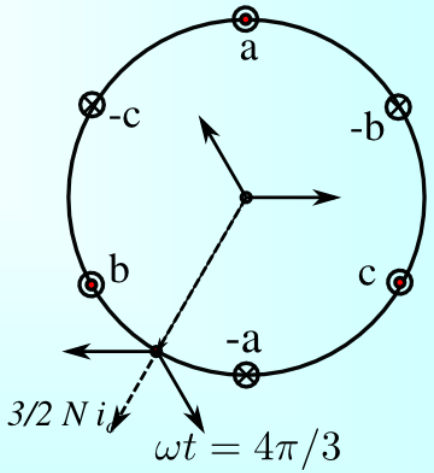




$\omega t = 0$

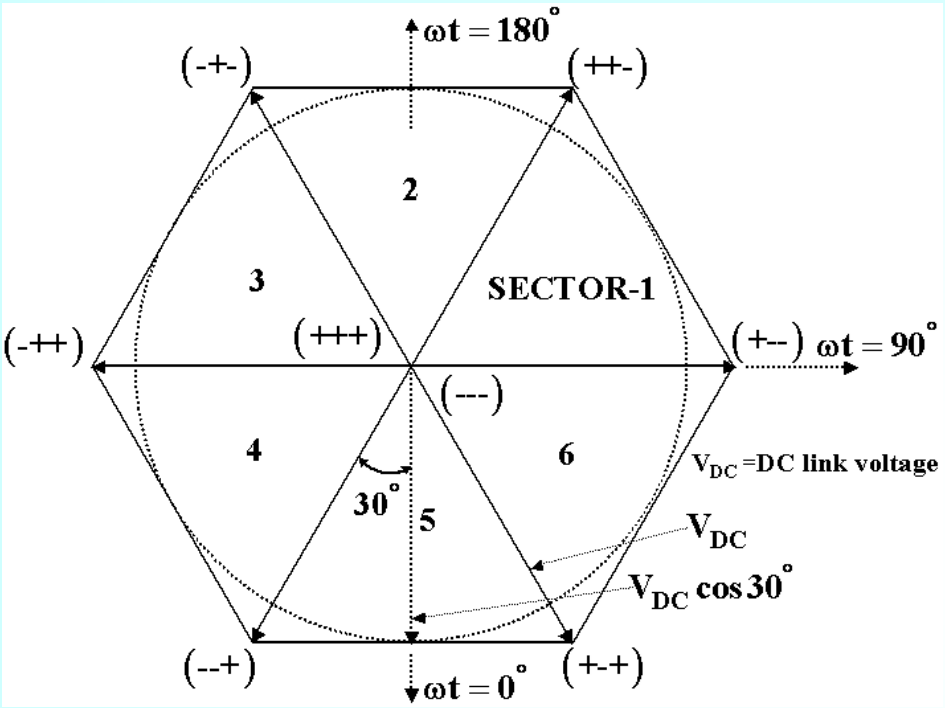


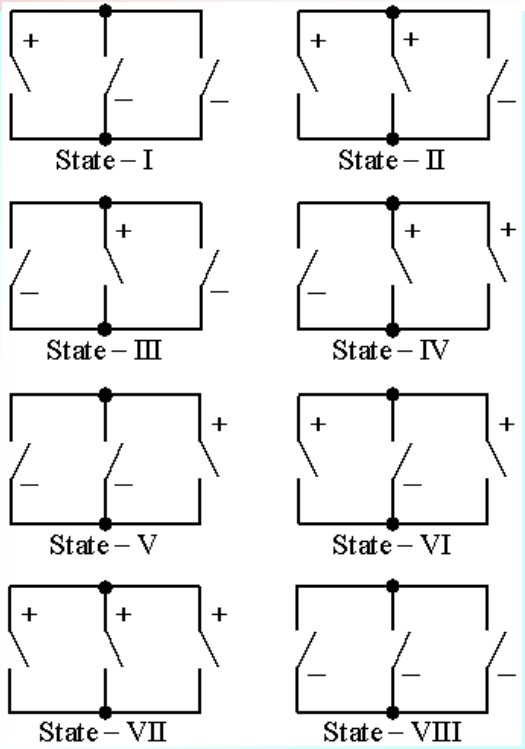
$\omega t = 2\pi/3$

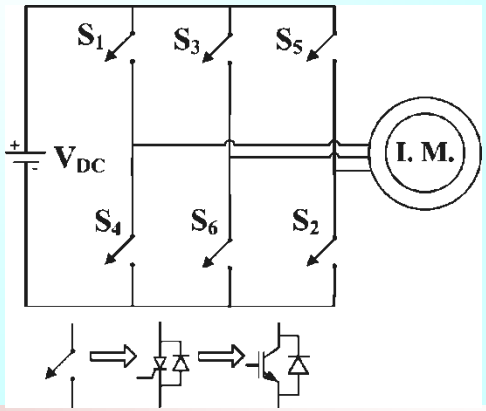


$\omega t = 4\pi/3$

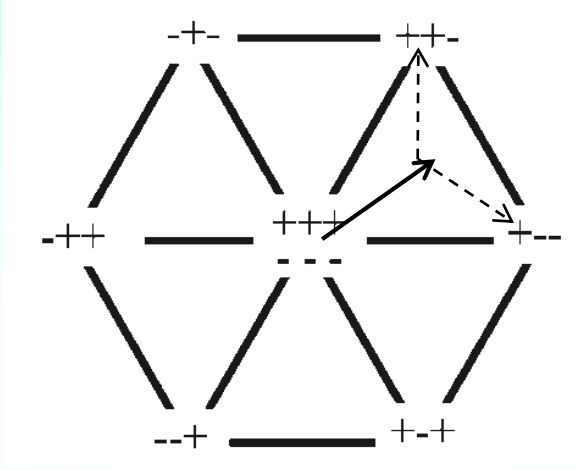
Vol tage space vector locations- 3-phase system







Space Vector Diagram



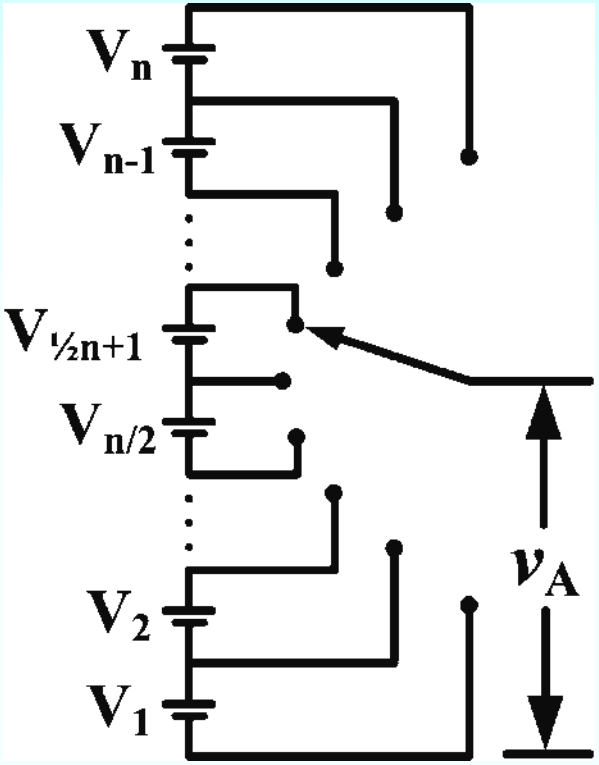
$$\mathbf{V_r} = v_{AO} + v_{BO}.\exp[j(2\pi/3)] + v_{CO}.\exp[j(4\pi/3)]$$

- Space vector (v_r) is nothing but a resultant representation all three phase voltage phasors in two-dimensional (α-β) plane
- The symbols '+' and '-' respectively indicate that the top switch and the bottom switch in a given phase leg are turned on

Multilevel Inverter topologies

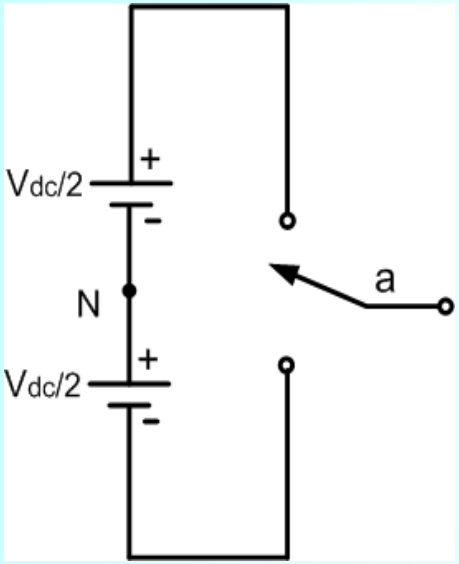
- The multilevel inverters are able to generate the output voltage with stepped waveform
- Better harmonic profile
- Less dv/dt
- It is possible to use power semiconductor devices of lower voltage ratings to realize higher voltage levels

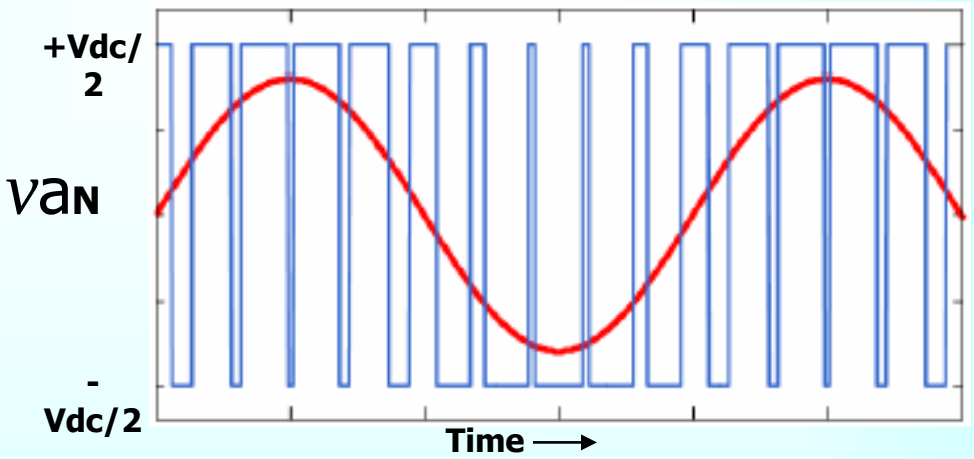
Schematic Diagram of Multilevel Inverter



- The symbol v_A represents the *pole voltage* of the inverter
- The pole voltage can be one of the *n* voltage magnitudes at any point of time
- These voltage magnitudes are generally referred as *levels*

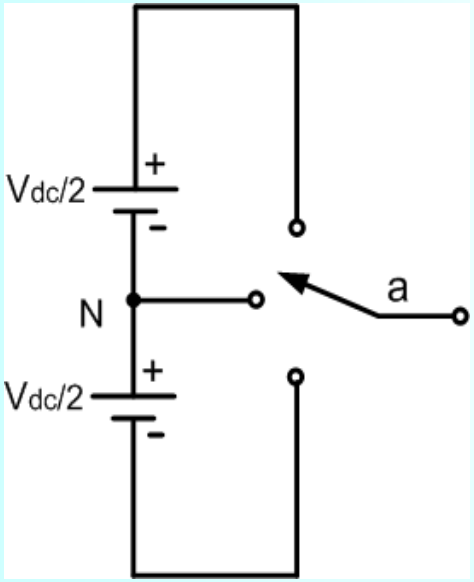
Two-level Inverter- SPWM

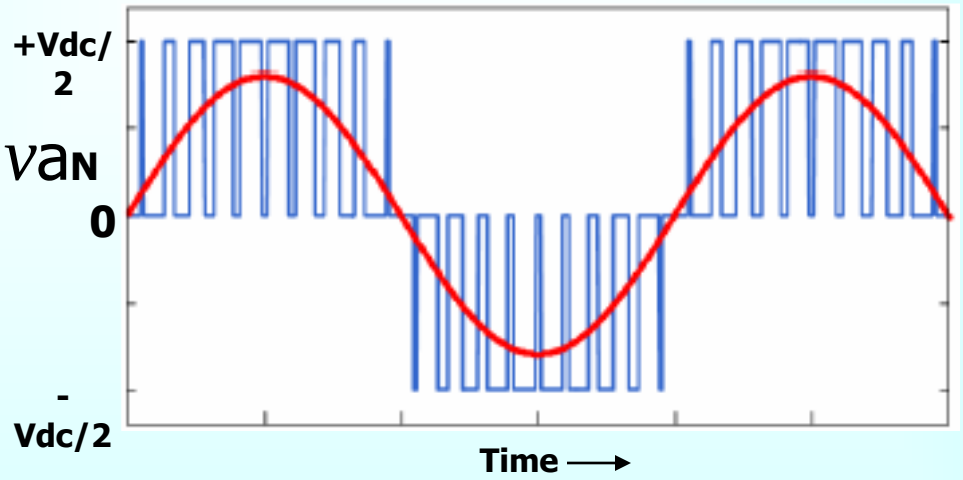




- Maximum magnitude can be up to Vdc.
- High dv/dt and associated EMI issues.
- High switching frequency is required

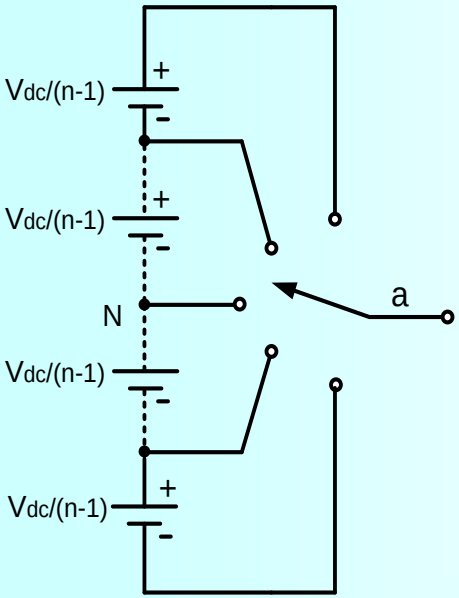
Three-level Inverter



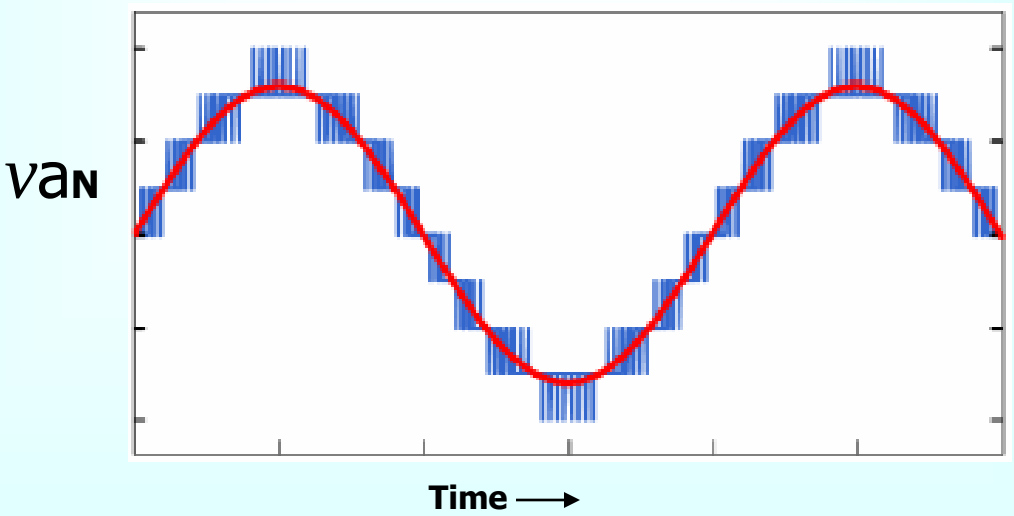


- Instantaneous error reduces in three level Inverter.
- Maximum magnitude can be up to Vdc/2.
- Hence harmonic distortion reduces.
- Reduction in dv/dt.

Multilevel Inverter



m-level

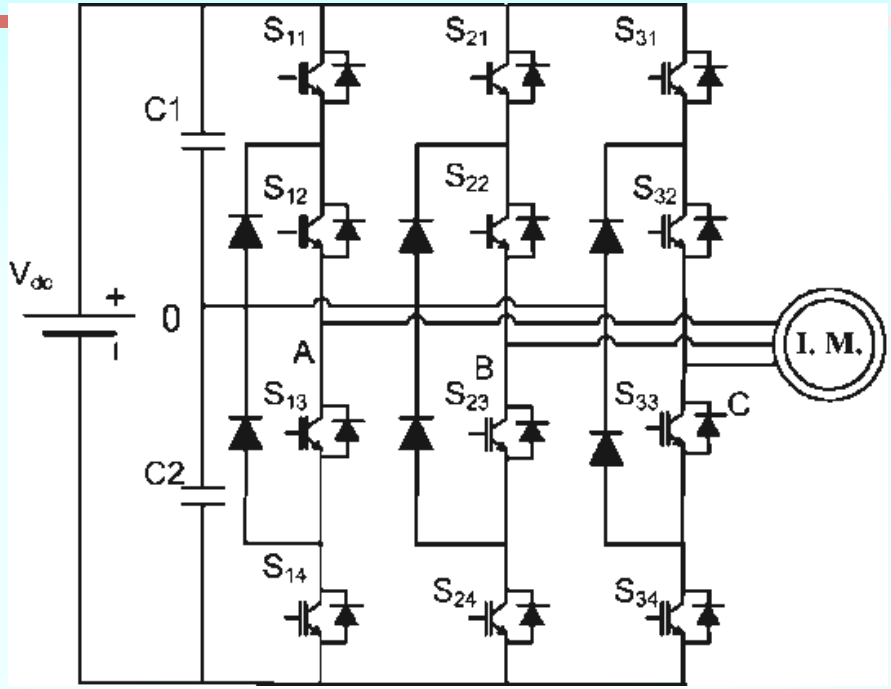


As the number of level increases instantaneous error decreases further.

Results in lower harmonic distortion and better waveform.

Nearly sinusoidal waveform can be generated at reduced switching frequency if the number of levels is high.

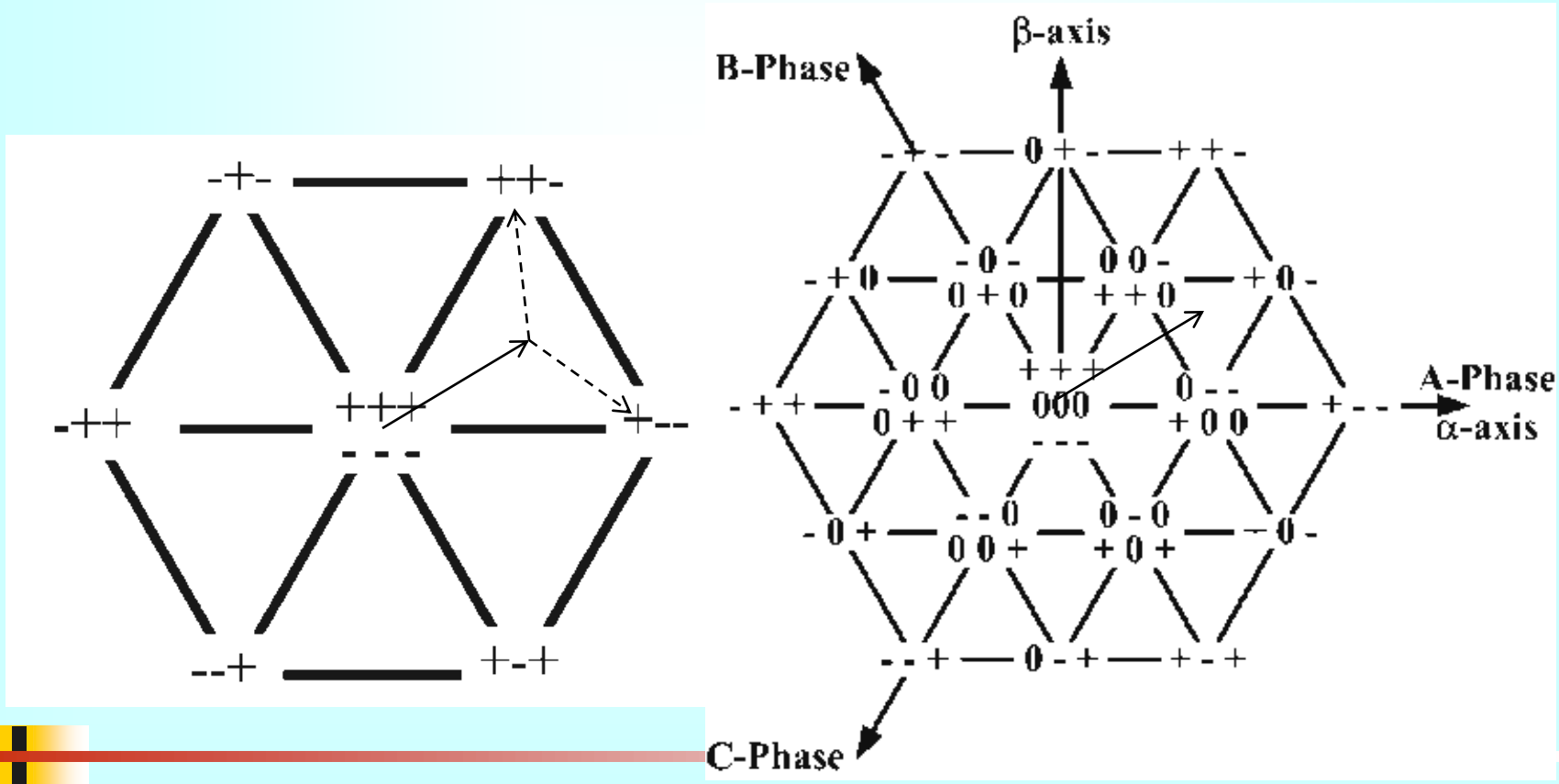
Neutral Point Clamped (NPC) Multilevel Inverter



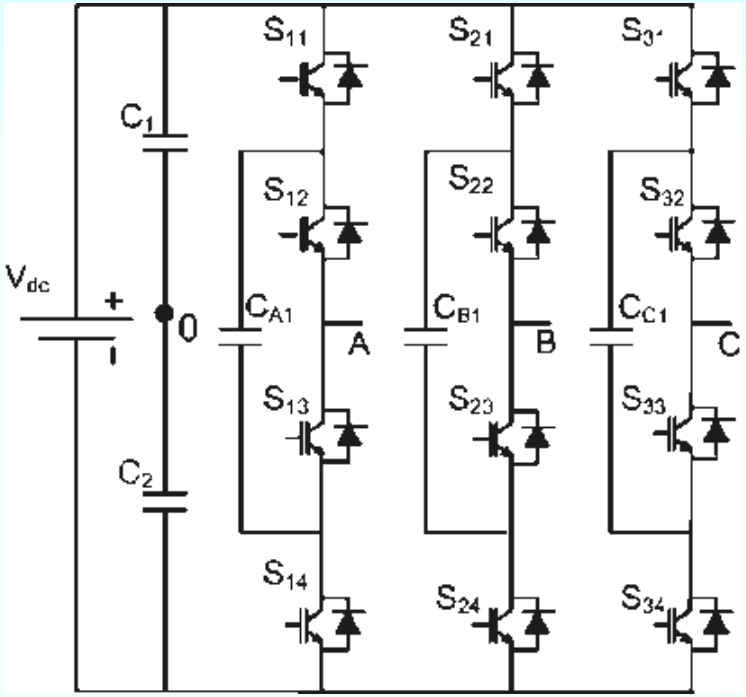
- Three-phase three-level NPC inverter has been proposed by Nabae, Takahashi and Akagi in the year 1981
- The dc-link voltage is split in to smaller voltage magnitudes using the series connected capacitor banks
- The middle point '0' of the two dc-link capacitors C_1 and C_2 is defined as a neutral-point

Voltage Space Vector Diagram of Three-Level Inverter

- Each pole voltage is capable of assuming 3 states independently of the other
- Total of 27 (3^3) are possible

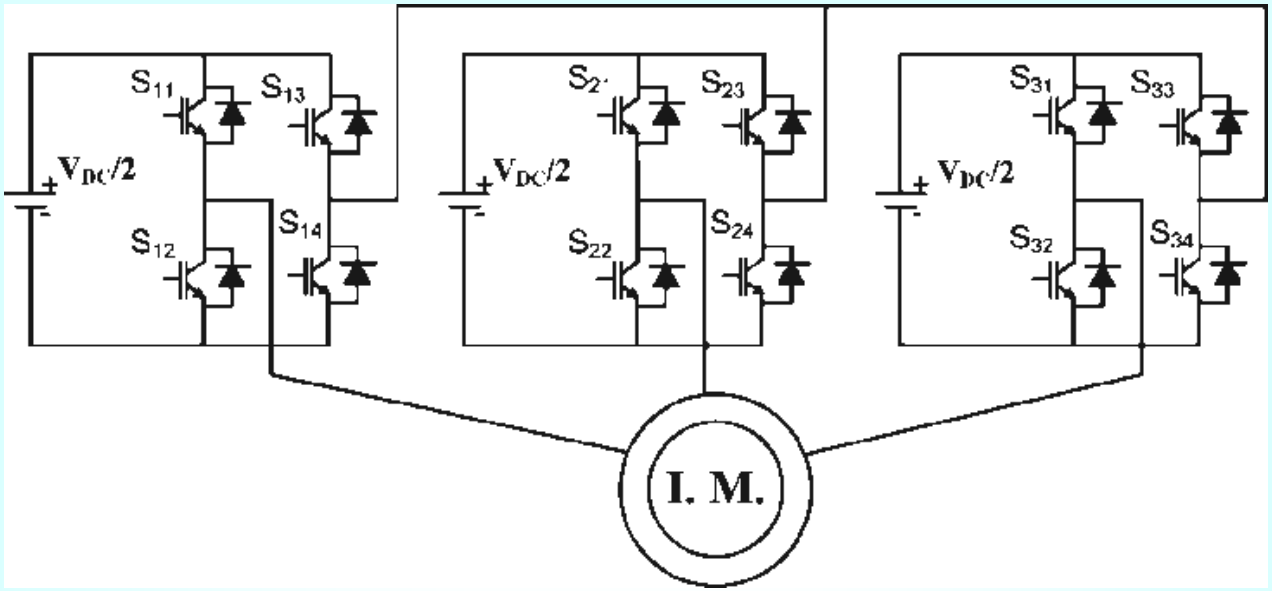


Flying capacitor (FC) multilevel inverter structures



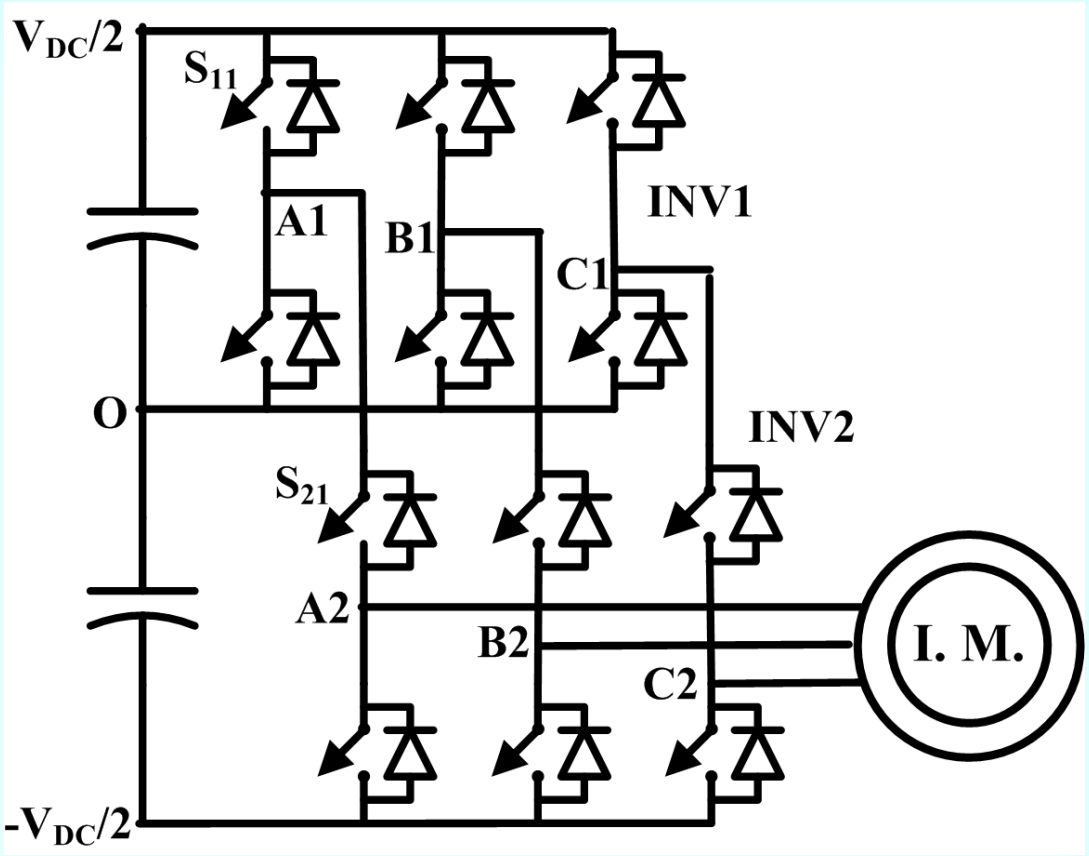
- The concept of flying capacitor multilevel inverter is introduced in the year 1992 by T. A. Meynard and H. Foch
- The capacitor C_{A1} is charged to a voltage magnitude of $V_{dc}/2$

Cascaded H-bridge multilevel inverters



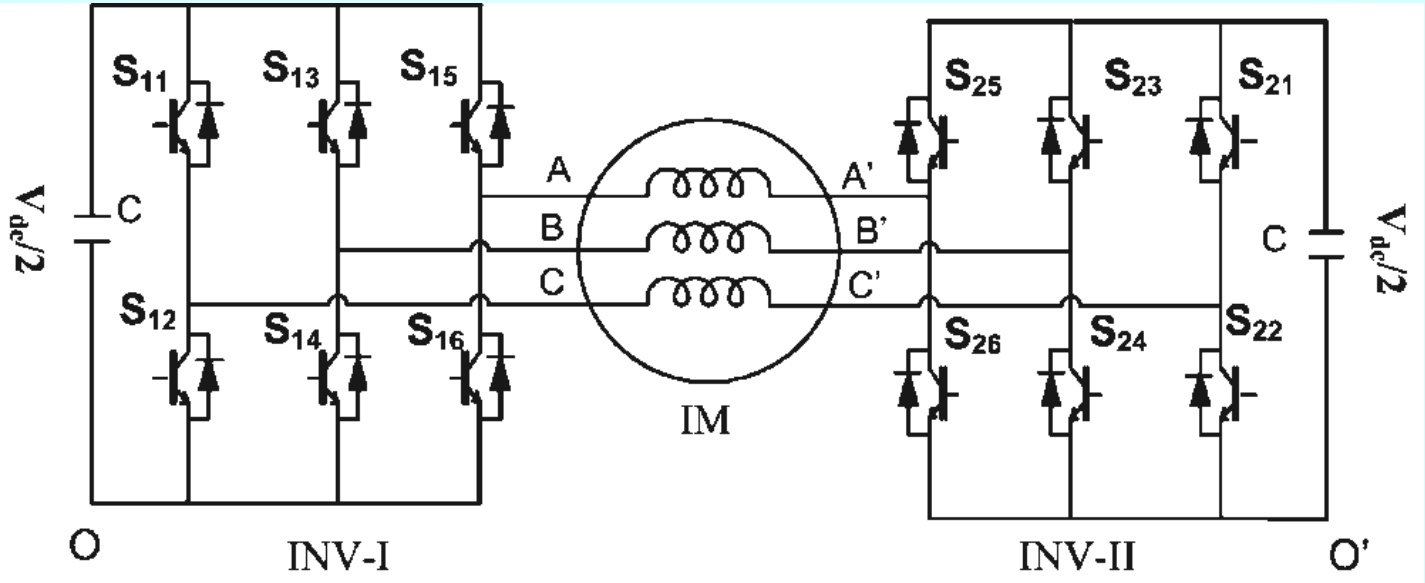
- The dc-link voltage magnitude required by the each cell in H-bridge inverter is $V_{dc}/2$ (i.e. half the magnitude compared to the NPC and FC inverter topologies)

Multi-level inverter configurations cascading conventional two-level inverters



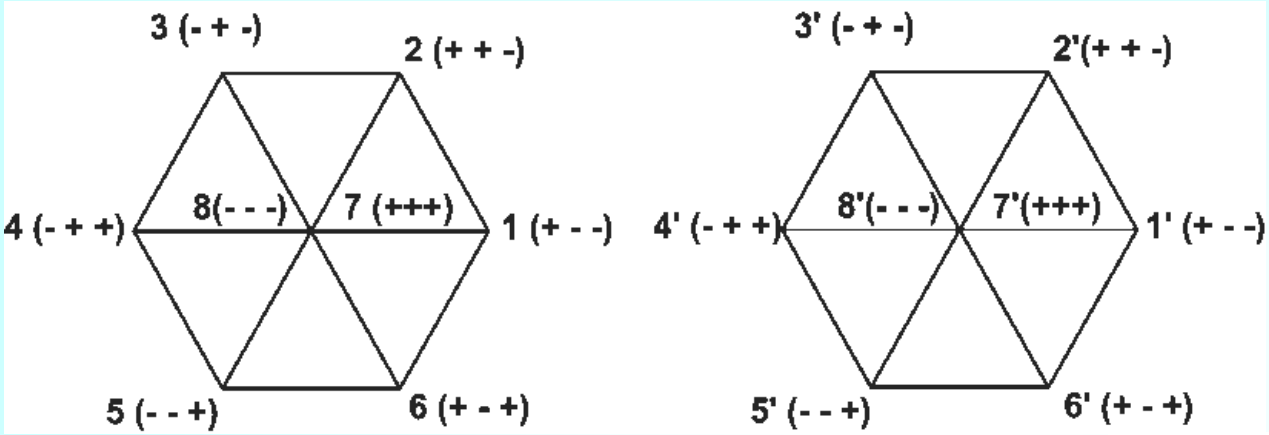
- The pole voltage v_{A2O} can be either $V_{dc}/2$, 0, or $-V_{dc}/2$

Three-level inverter topology for open-end winding induction motor

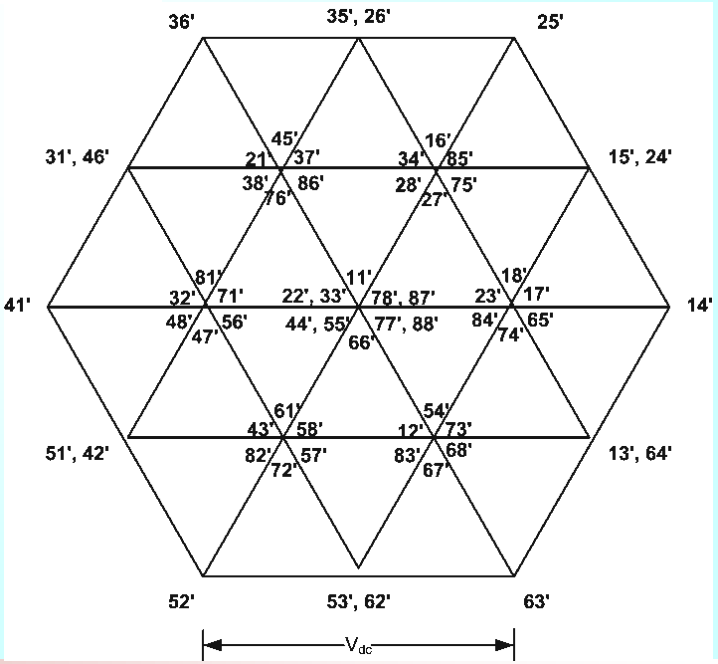


- The three-level inverter topology can be realized by feeding an open-end winding induction motor with two two-level inverter from both sides of the winding

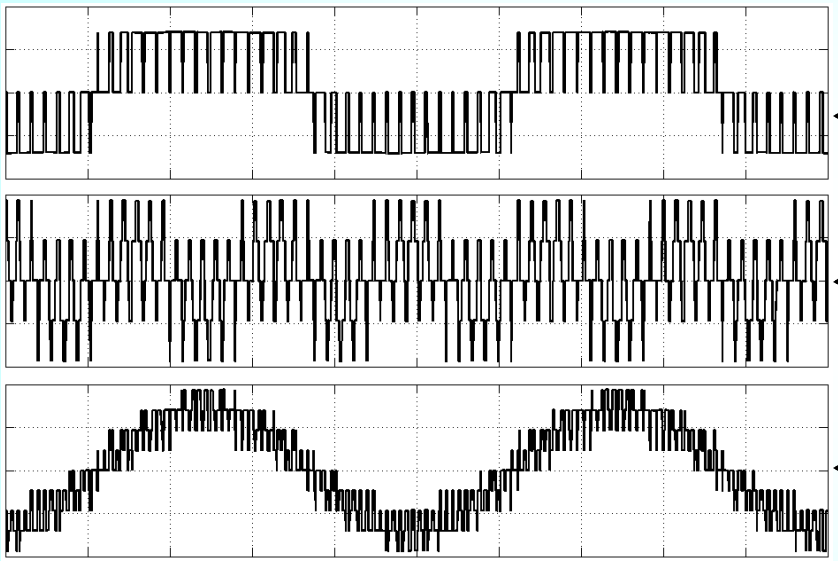
Switching states and voltage space vector locations of inverter-I and inverter-II



Switching states and space vector locations of open-end winding three level inverter



This multilevel inverter topology is free from capacitor voltage balancing issues



inverter pole voltage

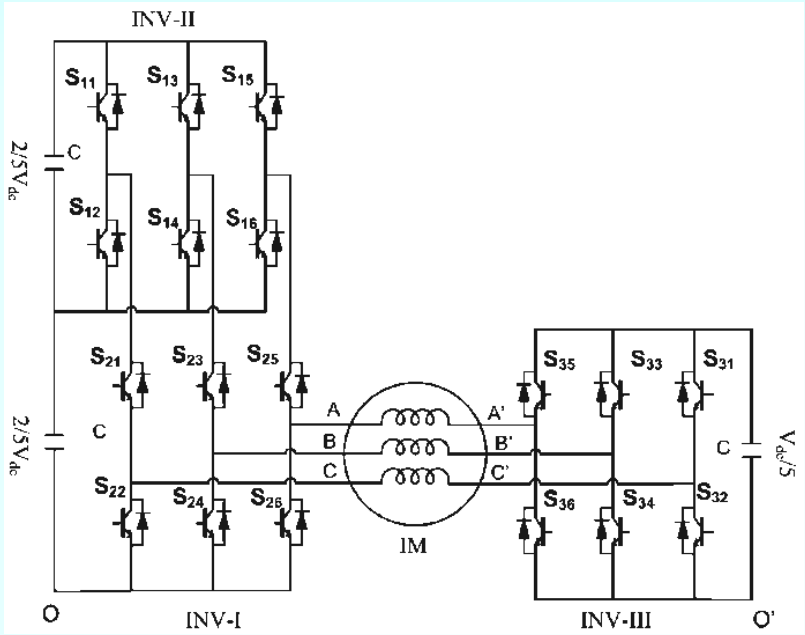
common mode voltage

phase voltage

Three-level inverter output voltages

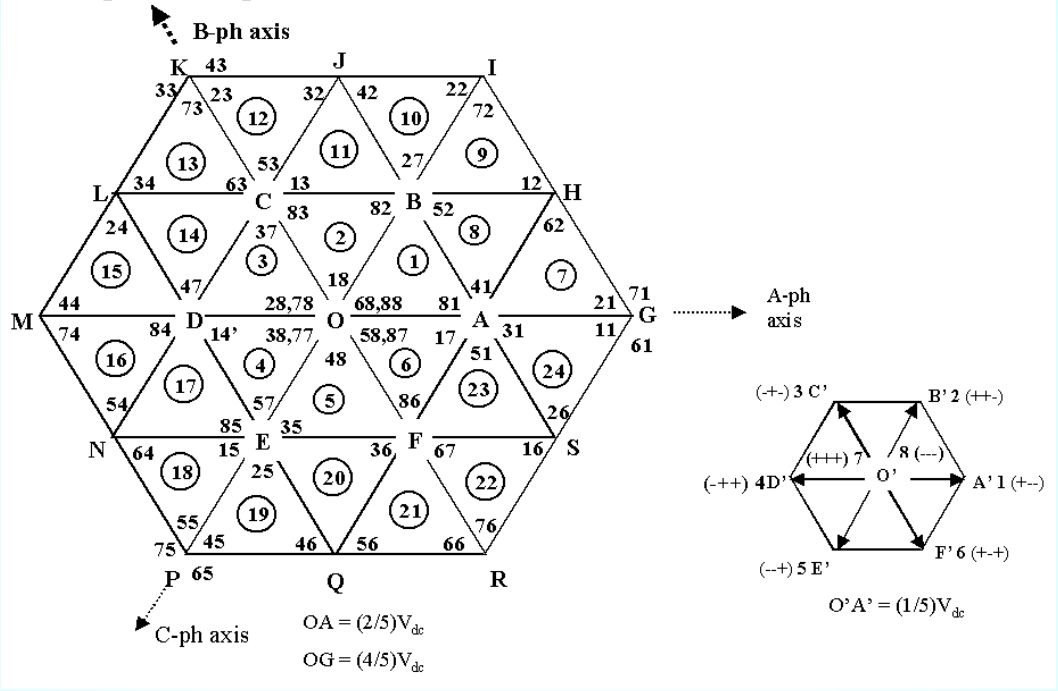
- The concept of open-end winding can be extended to higher number of voltage levels by cascading conventional two-level inverters, with or without asymmetrical dc voltages

Six-level inverter topology for open-end winding induction motor



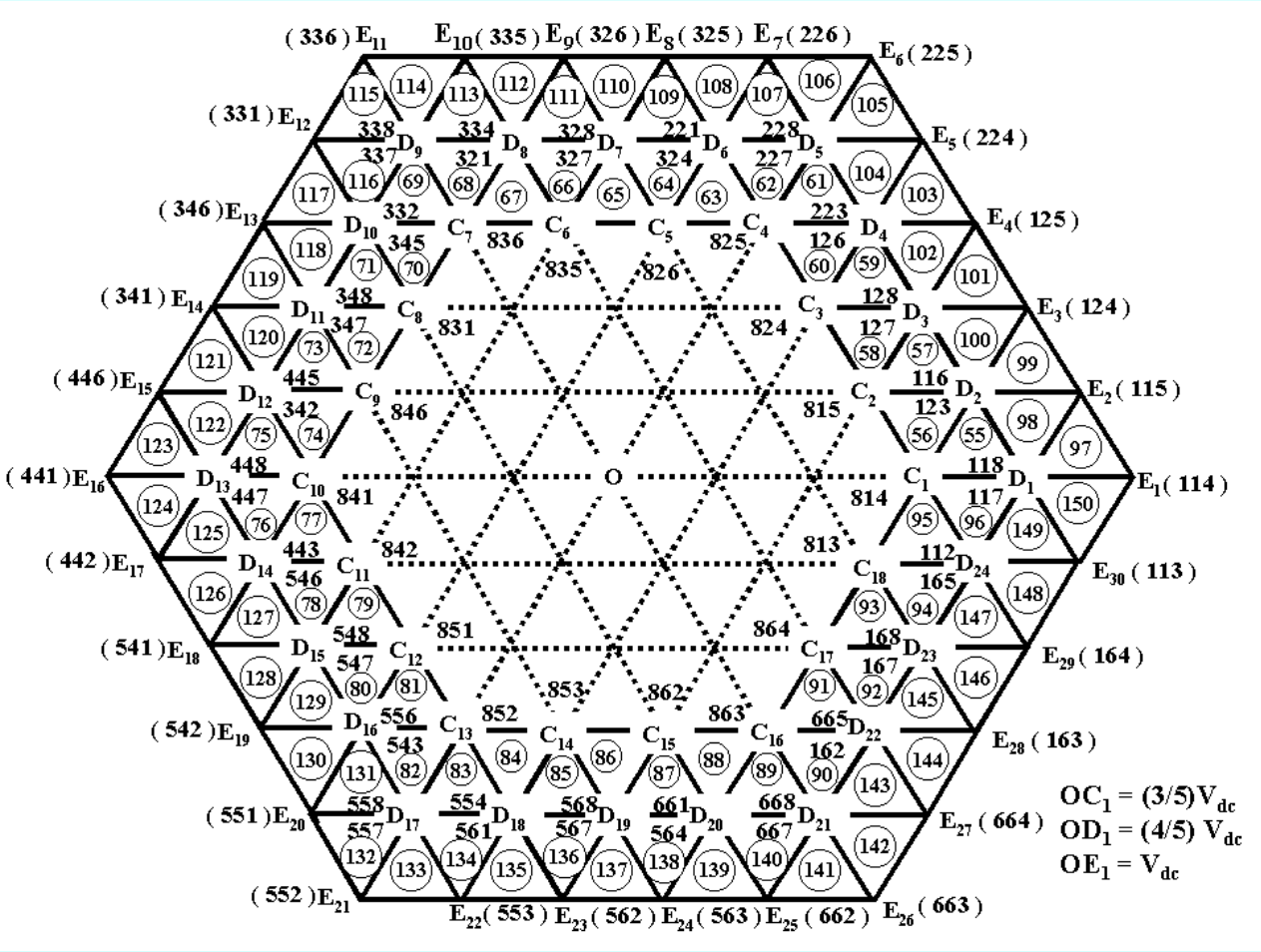
- The inverter-I and inverter-II are cascaded and fed with a voltage source of $2/5V_{dc}$
- Inverter-III is fed with a voltage source of $V_{dc}/5$
- This resultant inverter power circuit can generate six voltage levels on the motor phase windings by appropriately driving the switching devices
- The magnitudes of the six voltage levels are $-V_{dc}/5$, 0, $V_{dc}/5$, $2V_{dc}/5$, $3V_{dc}/5$ and $4V_{dc}/5$

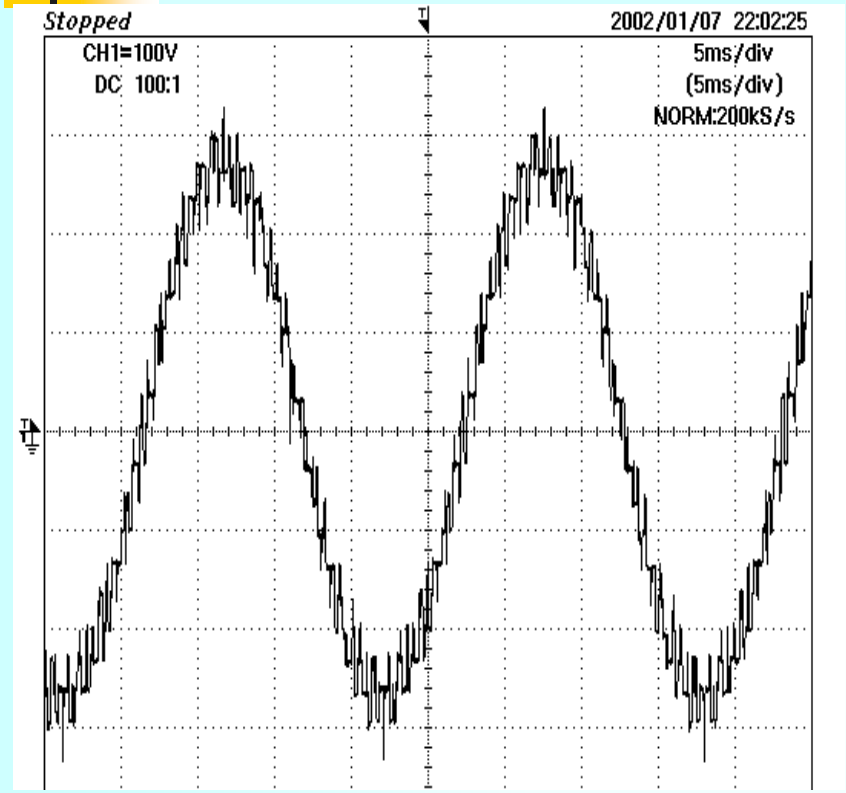
Voltage space vector locations of the three-level inverter (Left) and the two-level inverter (Right)

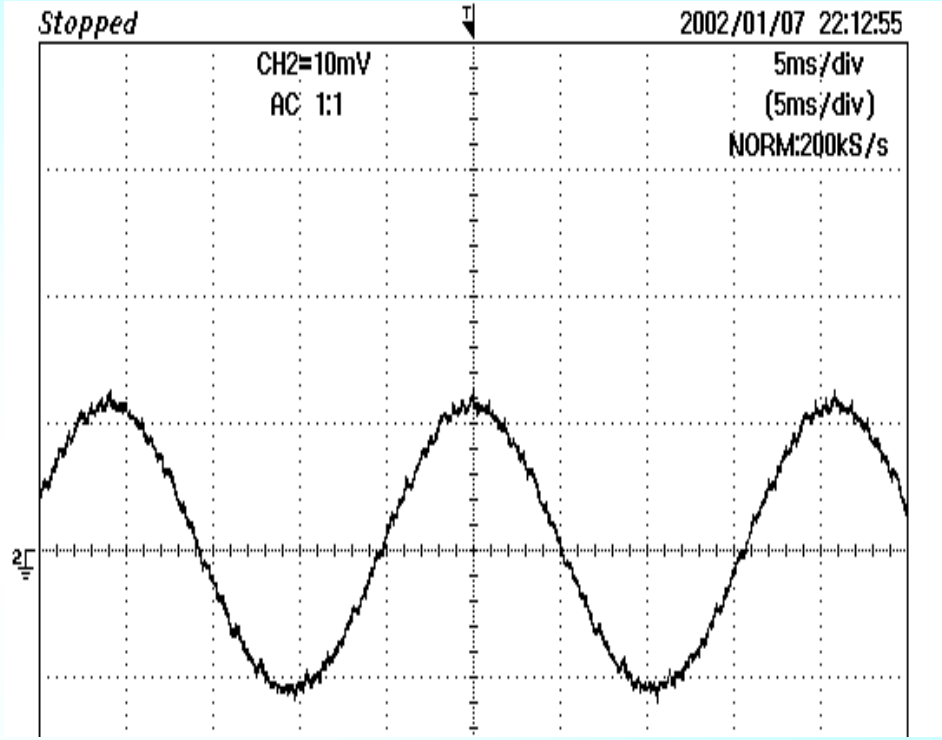


- It may be noted that the three-level inverter has 64 space vector combinations, due to the cascaded effect of inverter-1 and inverter-2, distributed over 19 space vector locations
- The two-level inverter has 8 space vectors distributed over 7 locations

The voltage space vector locations for the six-level inverter topology

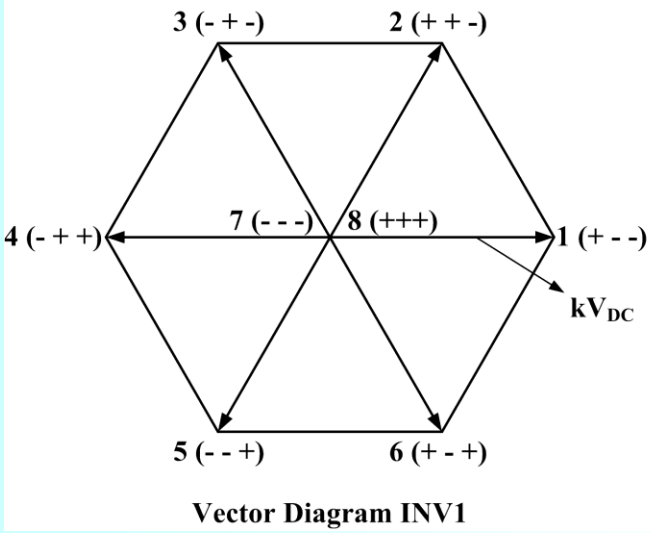




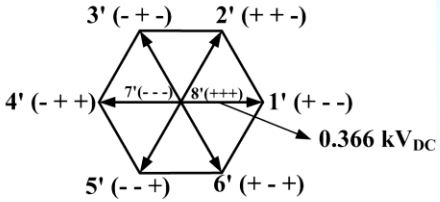


- The motor phase voltage and phase current at M=0.83
- At this modulation index the inverter is operating in six-level mode

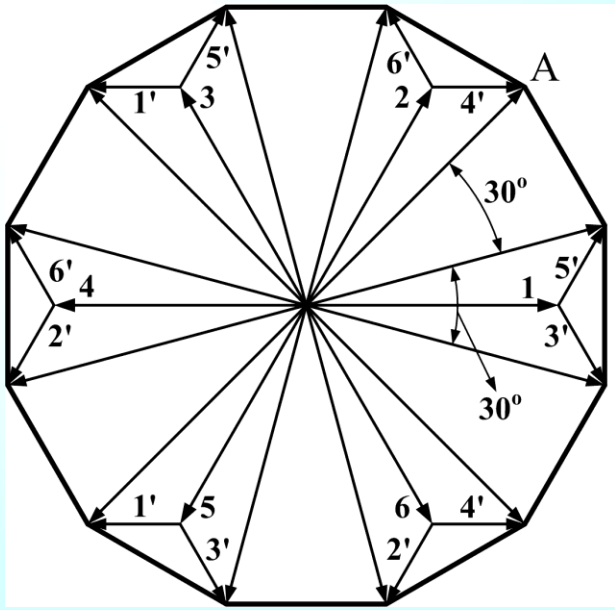
Basic 12-sided polygonal space vector diagram realization



Vector Diagram INV1

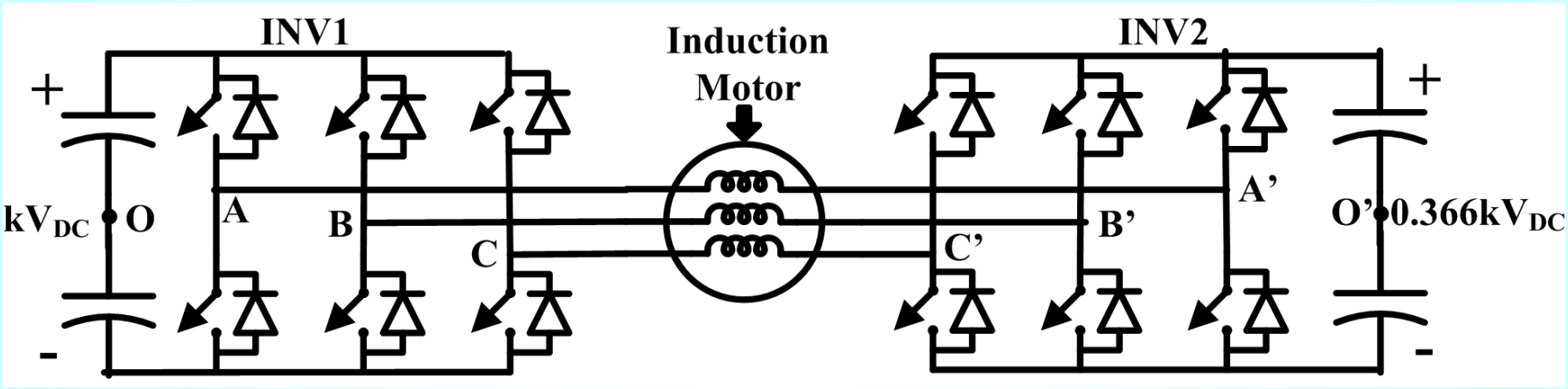


Vector Diagram INV2



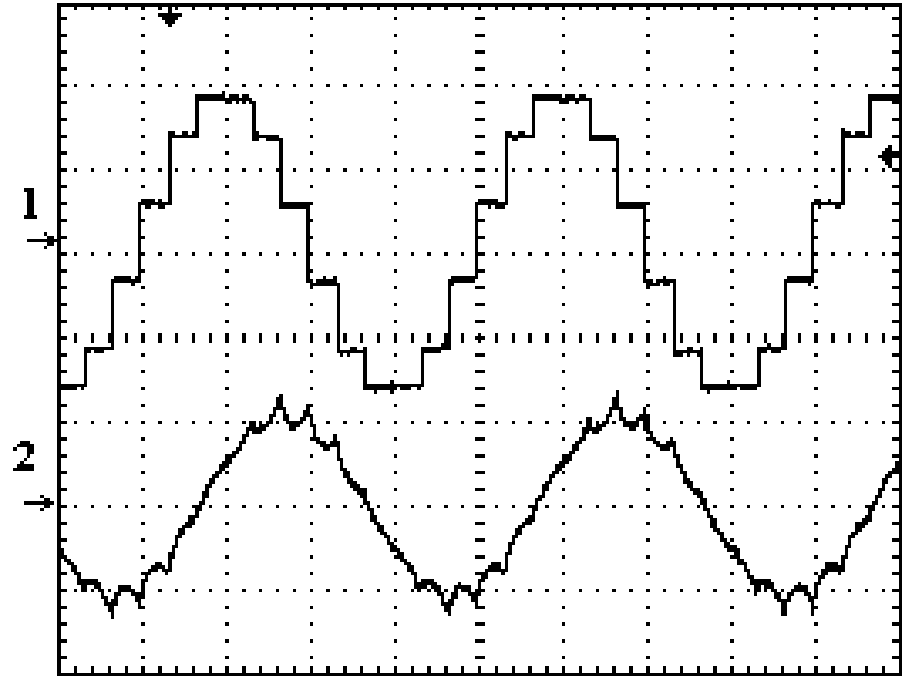
1, 1'→ (+ - -)
2, 2'→ (+ + -)
3, 3'→ (- + -)
4, 4'→ (- + +)
5, 5'→ (- - +)
6, 6'→ (+ - +)
7, 7'→ (- - -)
8, 8'→ (+++)

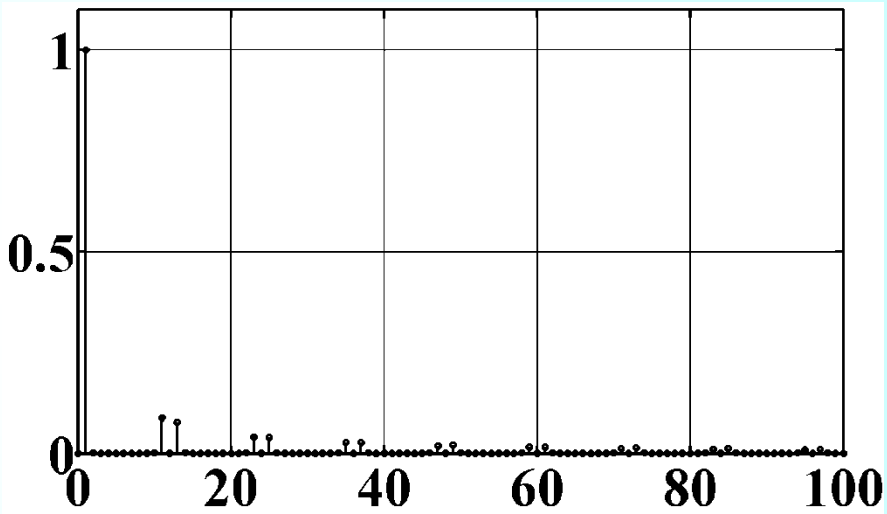
Power circuit realization



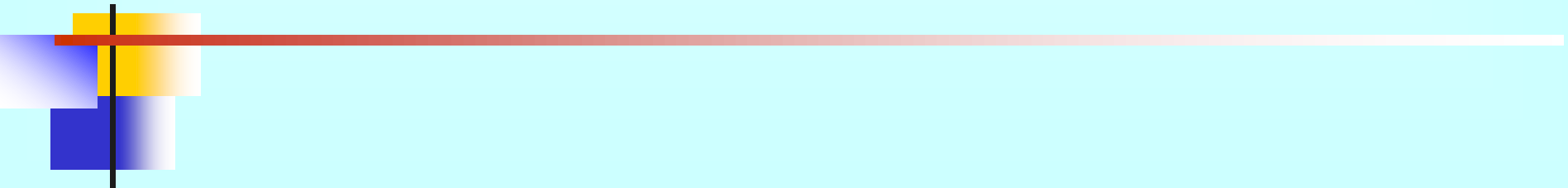
- Two 2-level inverters feed an open-end induction motor, but these two inverters are supplied from two isolated dc sources of magnitudes in the ratio 1:0.366
- Because of the asymmetry in the dc link, the hexagonal space vector diagram can be modified to form a 12-sided polygonal (*dodecagonal*) space vector diagram

Experimental result of phase voltage, its normalized harmonic spectrum and phase current



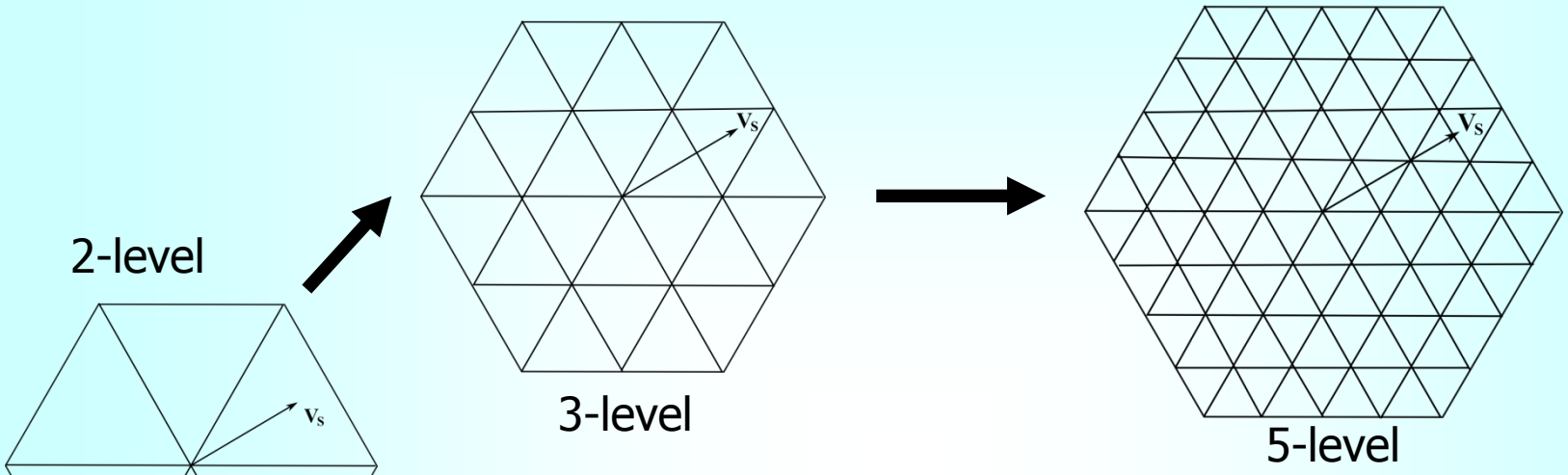


Investigations on Dodecagonal Space Vector Generation for Induction Motor Drives

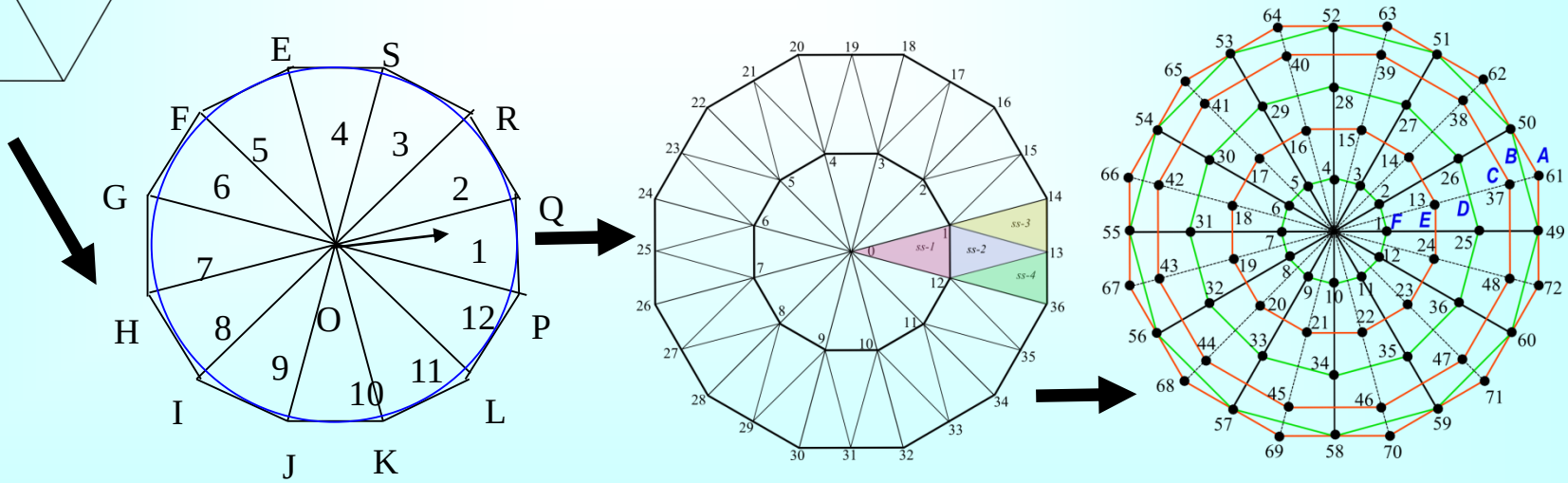


Evolution of space vector structures (Hexagonal and 12-sided)

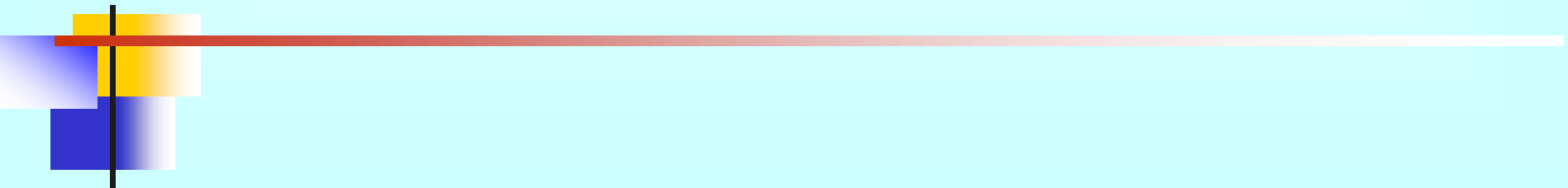
Hexagonal space vectors.



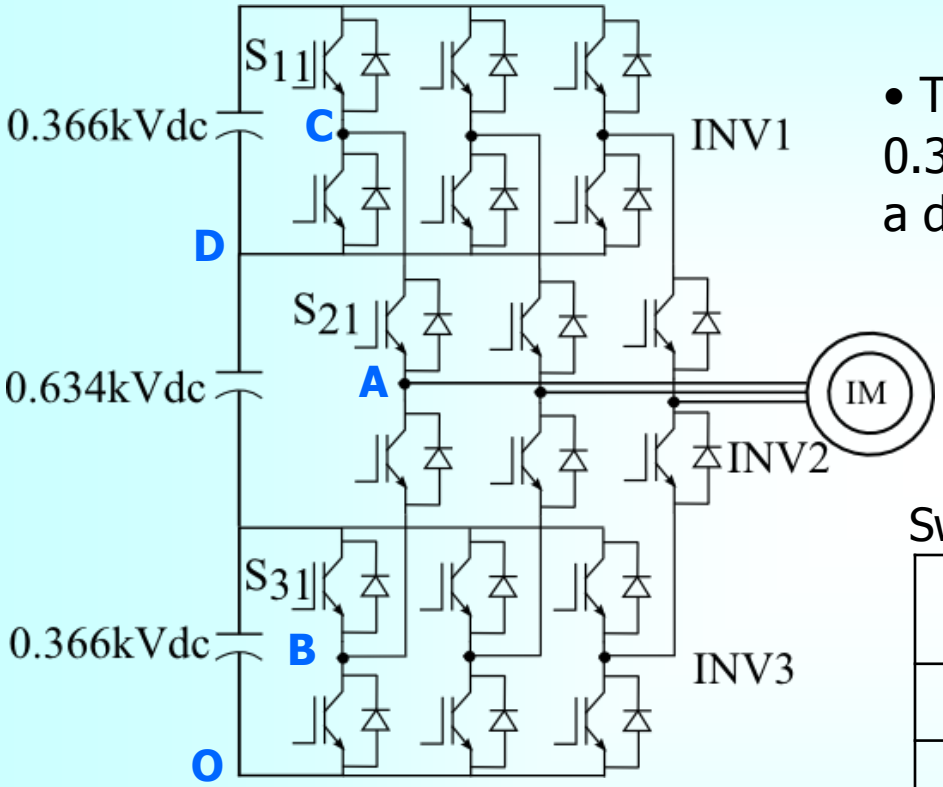
12-sided polygonal space vectors.



Part-1
A Combination of Hexagonal and Dodecagonal Voltage Space Vector Diagram for Induction Motor Drives



Topology of a multilevel inverter for generation of 12-sided polygonal voltage space vector



Pole voltage of overall inverter- v_{AO}
Pole voltage of INV3- v_{BO}
Pole voltage of INV2- v_{AB}
Pole voltage of INV1- v_{CD}

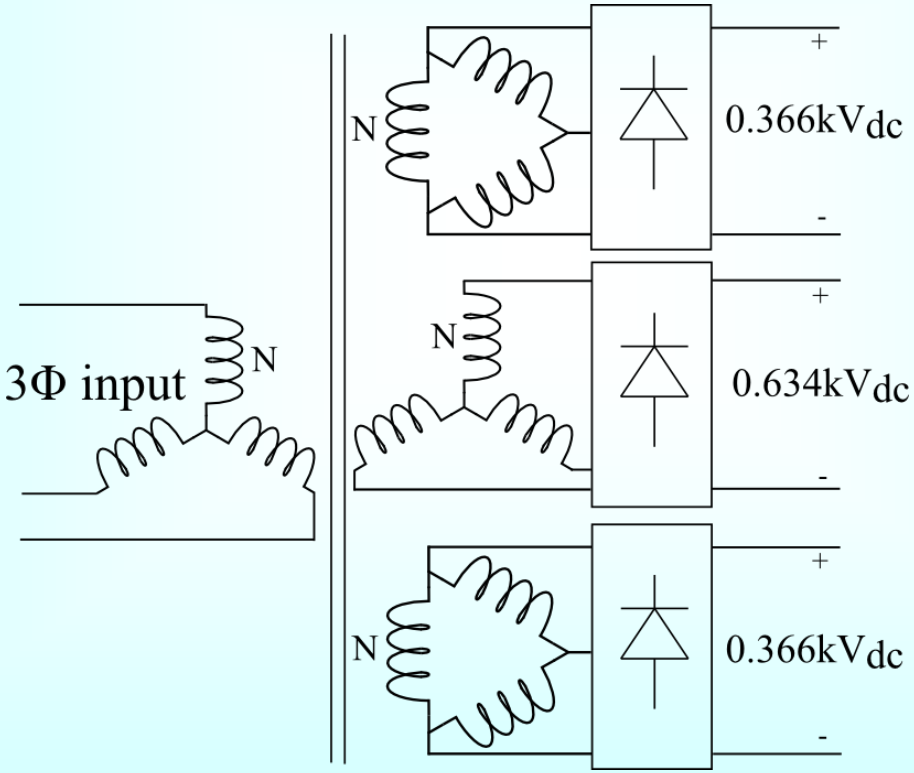
- Consists of three cascaded 2-level inverters
- Two inverters are supplied with a dc bus of 0.366kVdc while the third one is supplied with a dc bus of $0.634kV_{dc}$.

Switch status for different levels of pole voltage

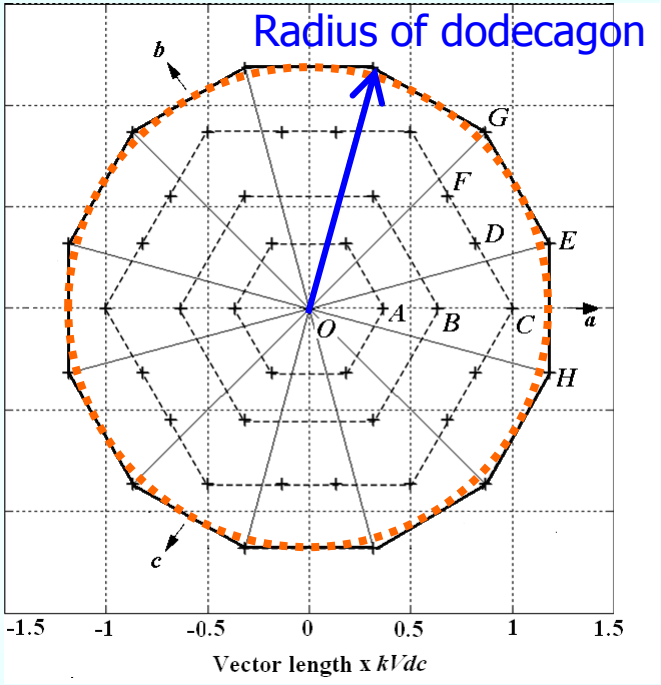
		R-phase		
Pole voltage	Level	S11	S21	S31
$1.366kV_{dc}$	**3**	1	1	1
$1.0kV_{dc}$	**2**	0	1	1
$0.366kV_{dc}$	**1**	1	0	1
$0V_{dc}$	**0**	1	0	0

Transformer connection for generation of 12-sided polygonal voltage space vector

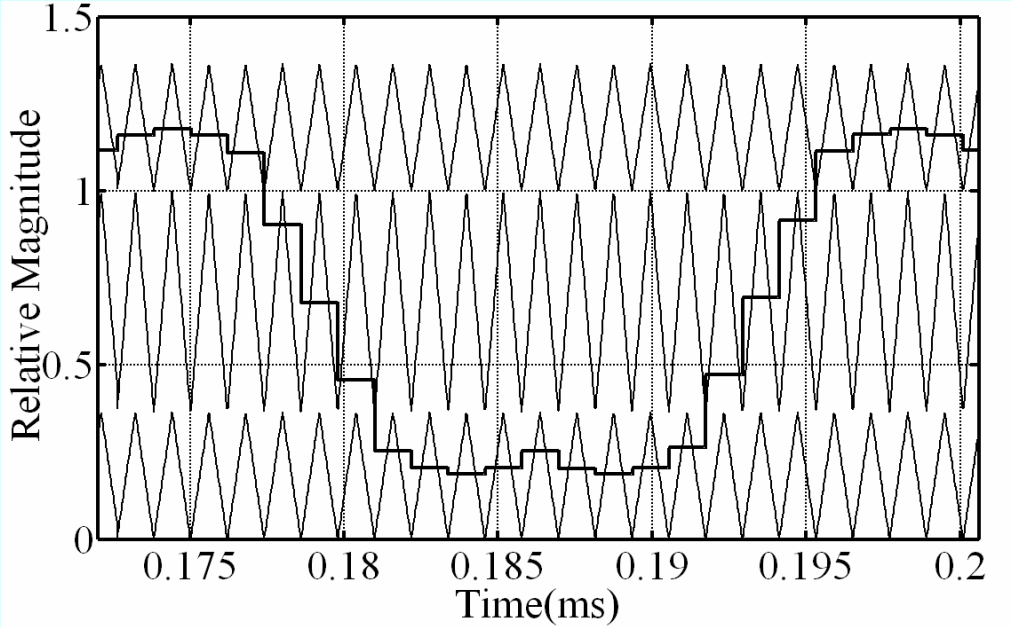
•Asymmetrical DC-links are easily realized by a combination of star-delta transformers, since $0.634kV_{dc}=\sqrt{3} \times 0.366kV_{dc}$.



Comparison with hexagonal space vector structure

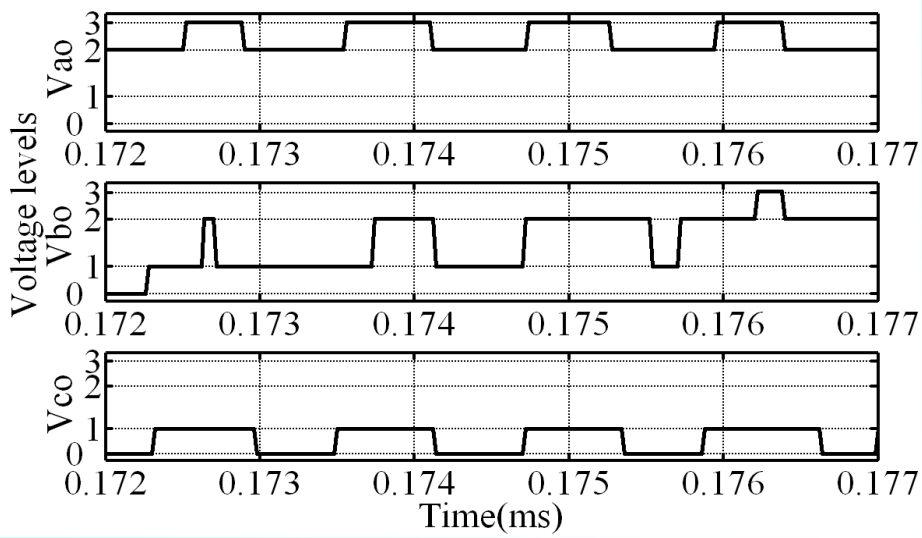


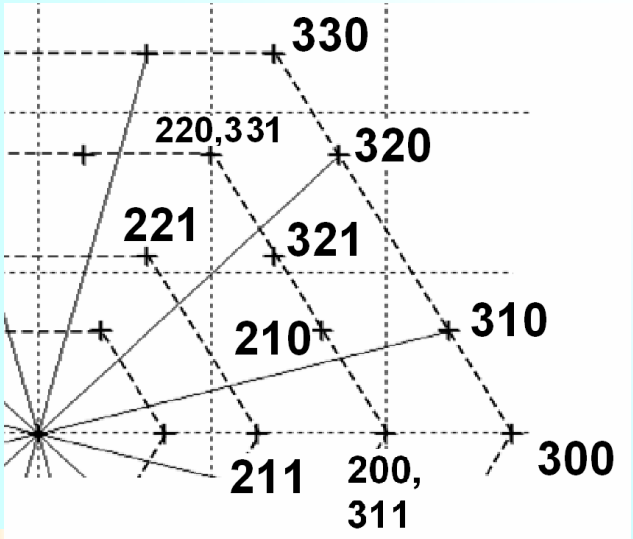
Modulating waveform



- The modulating waveform for phase-A for 35Hz operation (linear modulation range) is shown.
- The modulating waveform is synchronized with the start of the sector (sampling interval is always a multiple of twelve).
- Because of asymmetric voltage levels, three asymmetric synchronized triangles are used; their amplitudes are in the ratio 1:√3:1.

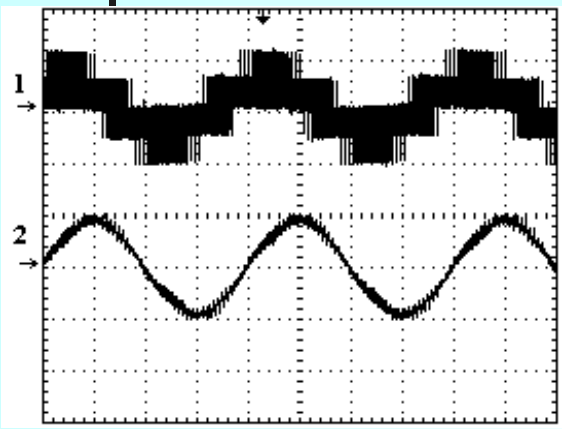
Switching sequence analysis





- Three pole voltages are shown for a 60 degree interval at 35Hz operation.
- In 'A' phase the voltage level fluctuate between levels '*3*' and '*2*', and in 'C' phase the voltage level fluctuates between levels '*1*' and '*0*'.
- The sequence in which the switches are operated are as follows: *(200), (210), (211), (311), (321), (311), (211), (210), (211), (311), (321), (211), (221), (321), (221), (210), (220), (221), (321), (331), (221), (220),* where the numbers in brackets indicate the level of voltage.
- This sequence corresponds to 2 samples per sector.

Experimental results-Operation at 10 Hz



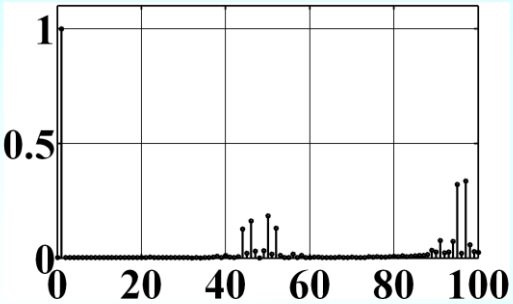
Phase voltage

Phase current

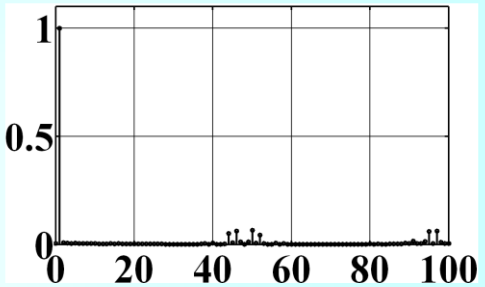
Phase voltage and current waveforms

Normalized harmonic spectrum of

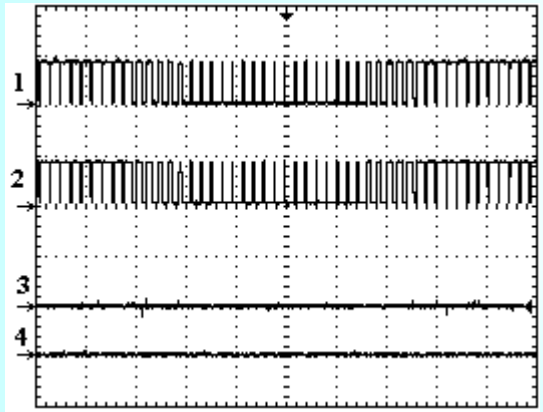
Phase voltage



Phase current



[Space Vector]



Overall inverter

INV3

INV2

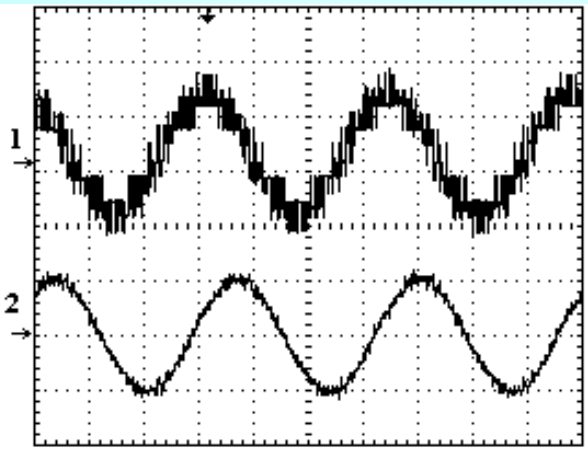
INV1

Pole voltage waveforms

- Switching happens within the innermost hexagon space vector locations.
- As seen from the pole voltage waveforms, only the lower inverter is switched while the other two inverters are off, hence the switching loss is low.
- Four samples are taken in each sector, so INV3 switching frequency is (12x4X10=480Hz). The first carrier band harmonics also reside around 48 times fundamental.

[Inverter Topology]

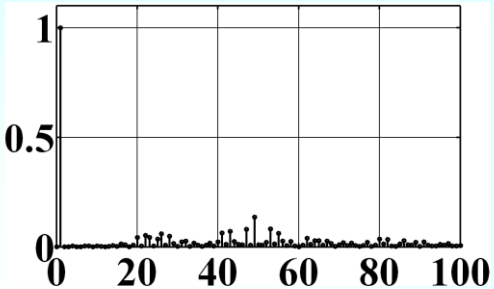
Experimental results-Operation at 30 Hz



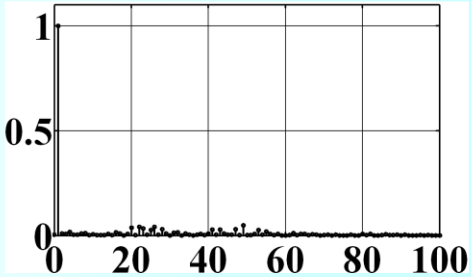
Phase voltage and current waveforms

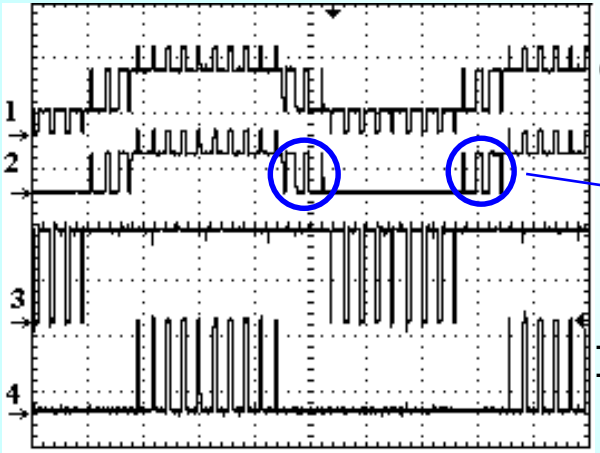
Normalized harmonic spectrum of

Phase voltage



Phase current



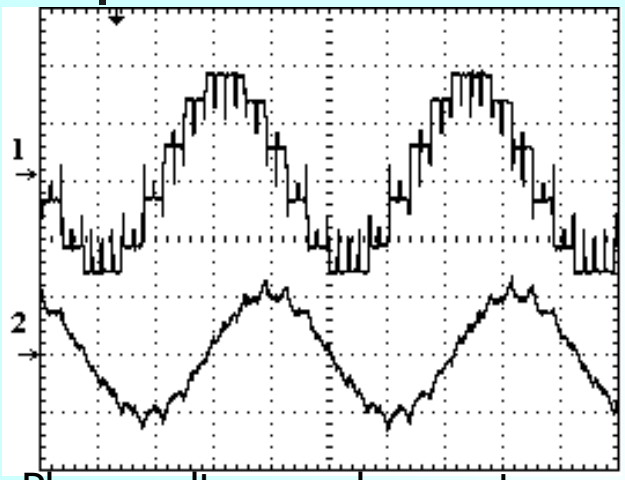


Pole voltage waveforms

- The space vector locations that are switched lie on the boundaries of the second and third hexagon from the center. [Space Vector]
- Number of samples are reduced from four to two, thus switching frequency is (f_s=12X2x30=720Hz).
- INV3 and INV1 are switched about 1/3rd of the total cycle, while INV2 is switched about 20% of the cycle.

[Inverter Topology]

Operation at 47 Hz (end of linear modulation range)



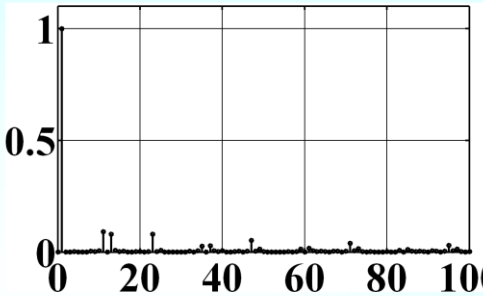
Phase voltage

Phase current

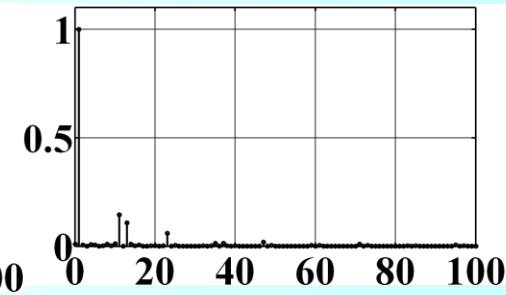
Phase voltage and current waveforms

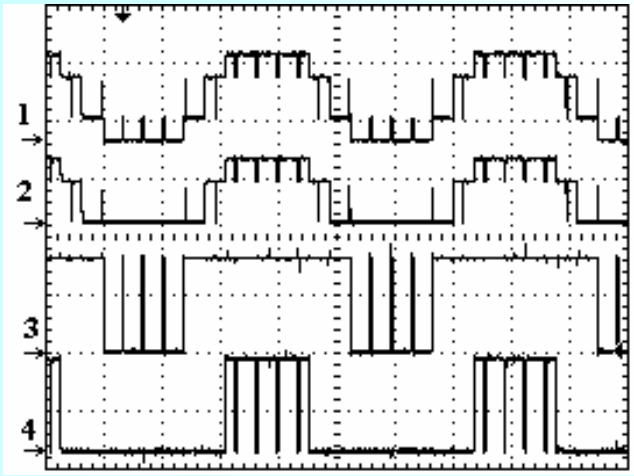
Normalized harmonic spectrum of

Phase voltage



Phase current





Overall inverter

INV2

INV3

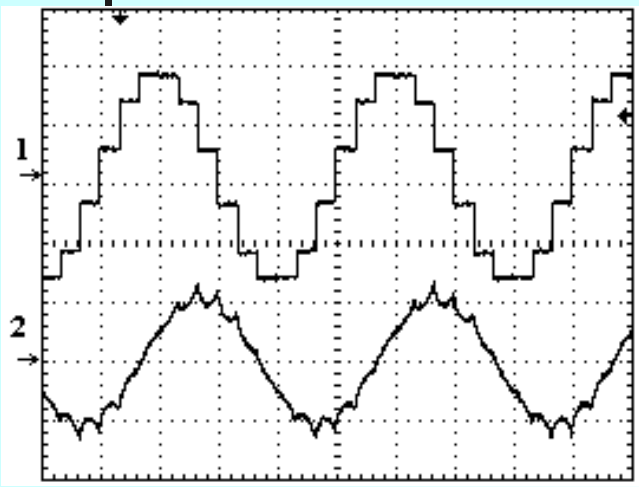
INV1

Pole voltage waveforms

- One sample is taken at the start of a sector, so switching frequency is only around (12X47=564Hz).
- The space vector locations that are switched lie between the outer hexagon and the 12-sided polygon.

[Space Vector]

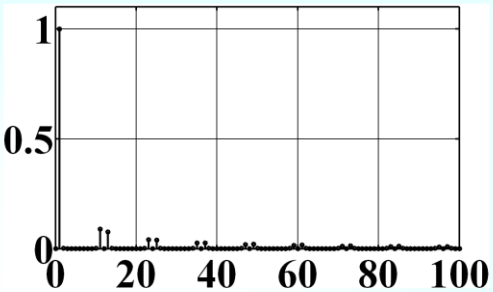
Operation at 50 Hz (12-step operation)



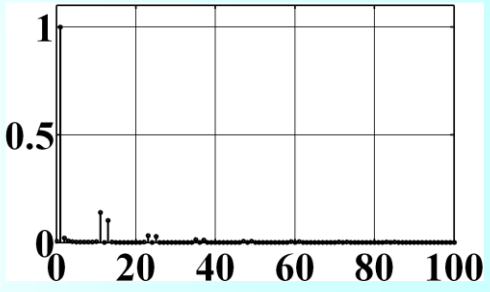
Phase voltage and current waveforms

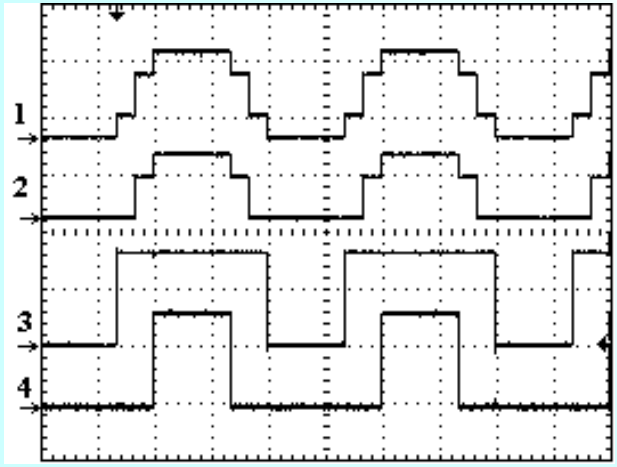
Normalized harmonic spectrum of

Phase voltage



Phase current



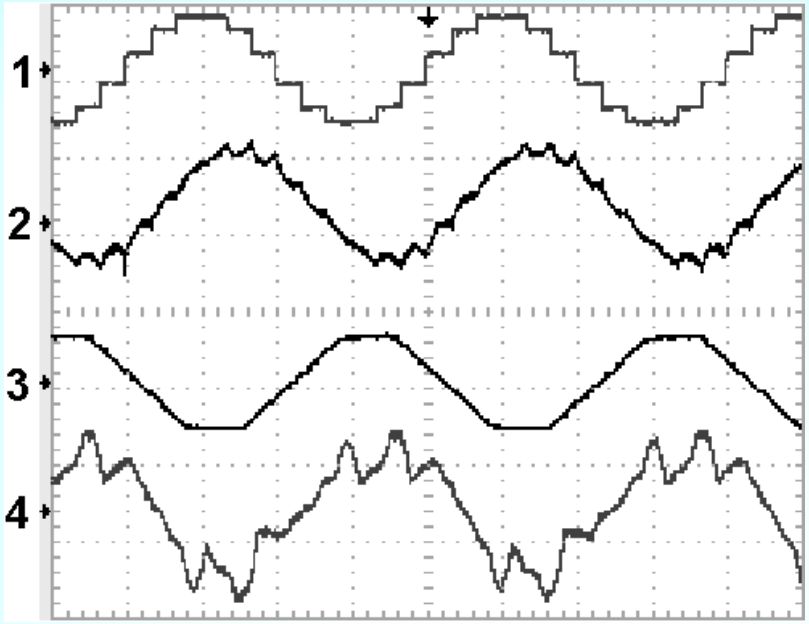


Pole voltage waveforms

- Complete elimination of 6n±1 harmonics (n=odd) from the phase voltage.
- One sample is taken at the start of a sector (f_s=12X1x50=600Hz).
- Each inverter is switched only once in a cycle.

Inverter Topology

Input current at 50 Hz (12-step operation)



Phase voltage

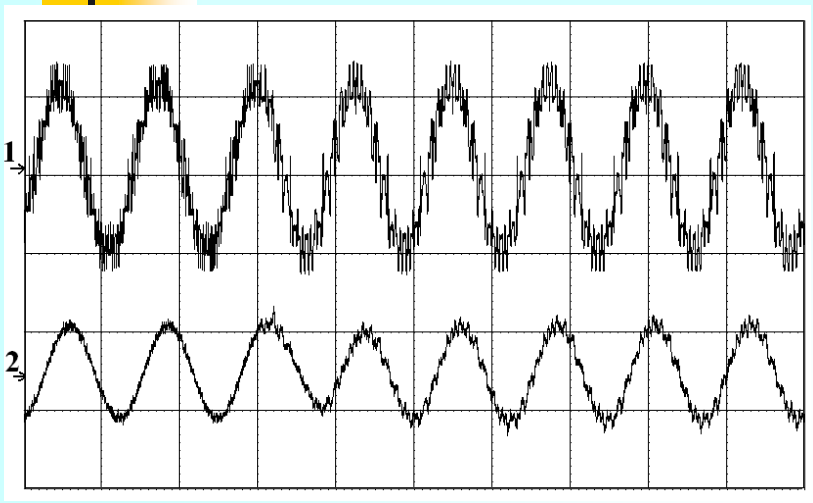
Phase current

Input phase voltage

Input line current

- The input current to the inverter is not peaky in nature, because of the presence of the star-delta transformers.

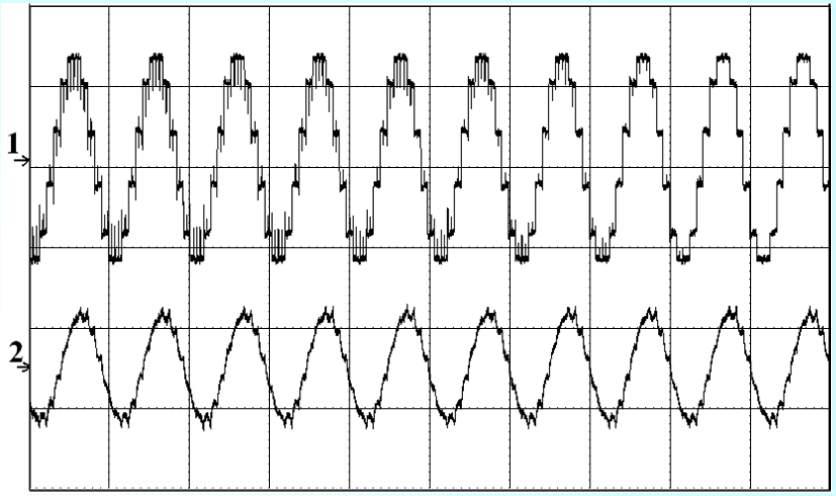
Motor acceleration with open loop V/f Control



Transition of motor phase voltage and current from 24 samples to 12 samples per cycle at 40Hz

Phase voltage

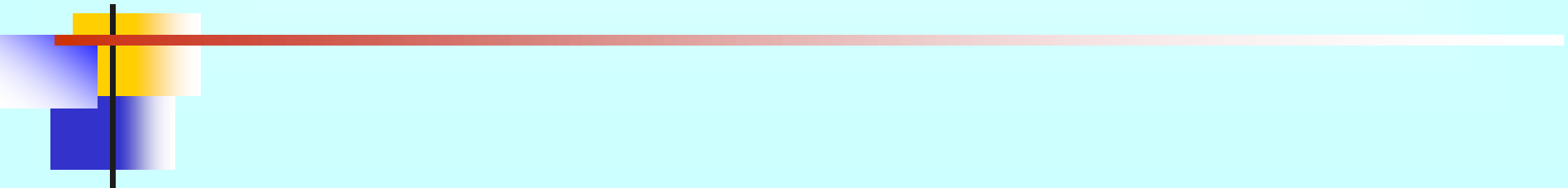
Phase current



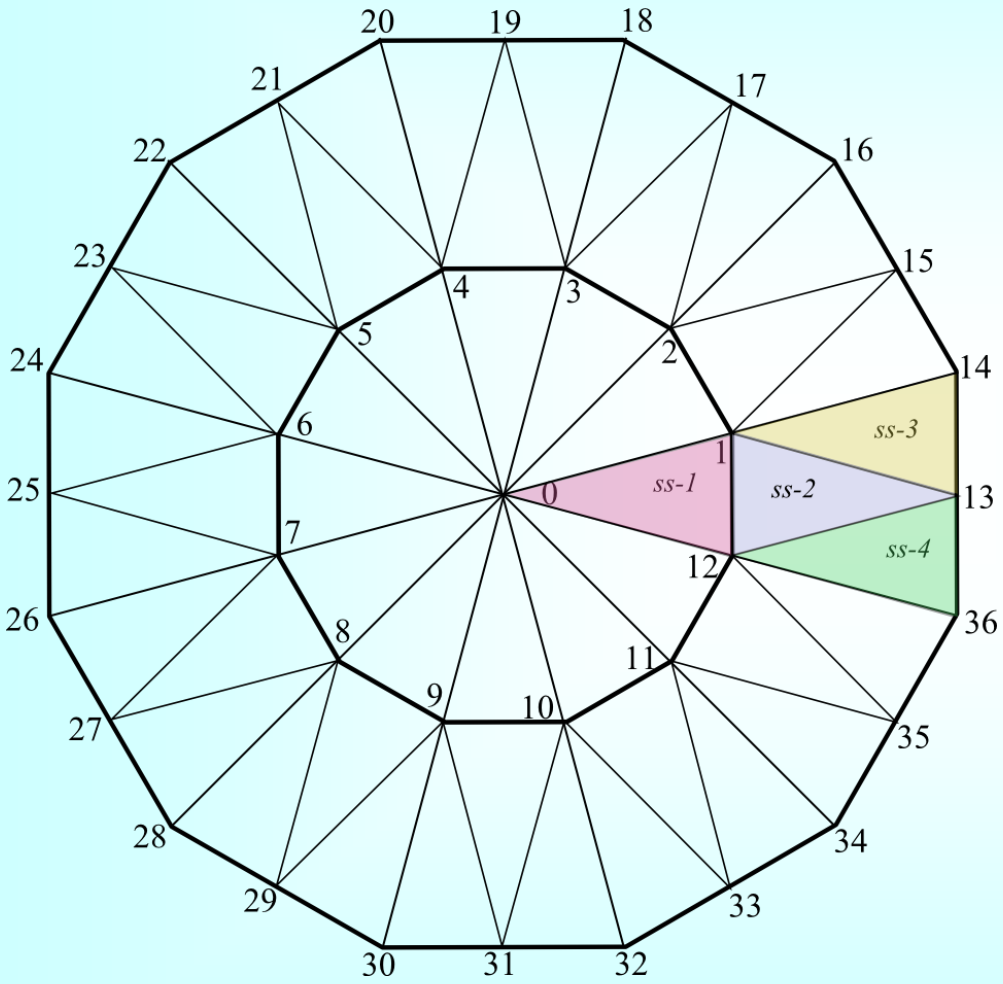
Transition of motor phase voltage and current from outermost hexagon to 12-step operation.

- Because of the suppression of the 5th and 7th order harmonics, the motor current changes smoothly during the transition when the number of samples per sector is reduced from two to one at 40Hz operation.
- As the speed of the motor is further increased, the inverter switching states pass through the inner hexagons and ultimately the phase voltage becomes a 12-step waveform.
- Under all operating conditions, the carrier is synchronized with the start of the sector.

Part-II
Generation of Multilevel Dodecagonal Space Vector Diagram

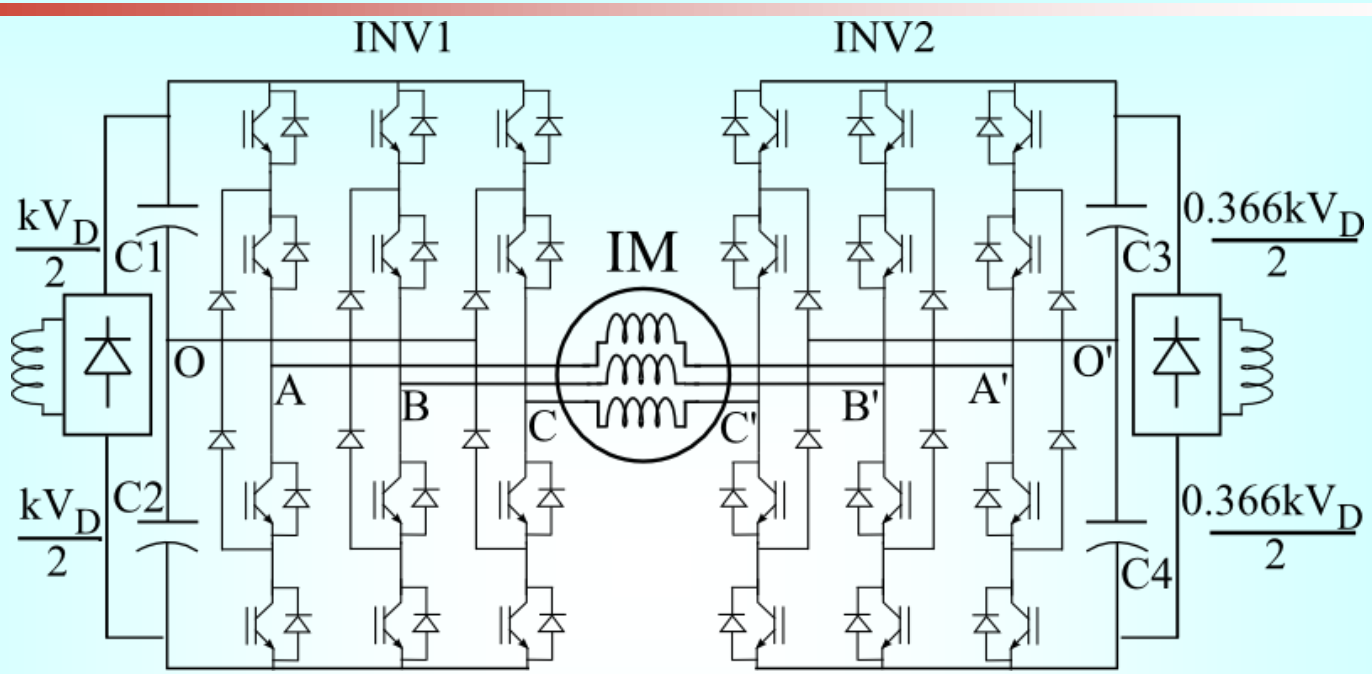


Multilevel 12-sided polygonal space vector structure



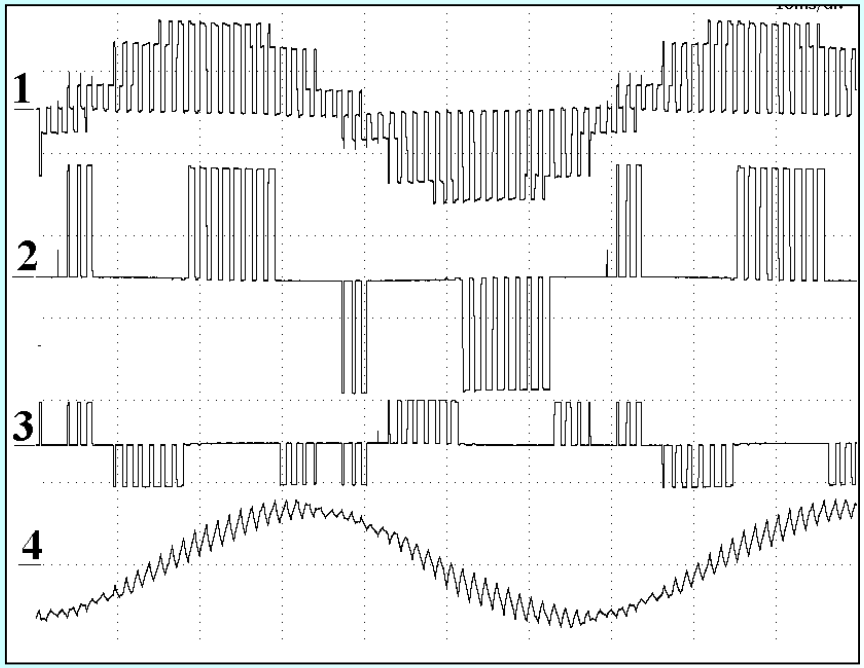
- Consists of two concentric 12-sided polygonal space vector structure.
- Unlike conventional hexagonal multilevel structure, here the sub-sectors are isosceles triangles rather than equilateral triangles.
- Each sector is thus divided into four sub-sectors as shown.

Inverter Structure



- In order to realize the proposed space vector structure, two conventional three level NPC inverters are used to feed an open ended induction motor.
- The two inverters are fed from asymmetrical dc voltage sources which can be obtained from the mains with the help of star-delta transformers and uncontrolled rectifiers.
- Because of capacitor voltage balancing of the NPC inverters, only two dc sources are used.

Experimental results-15 Hz operation



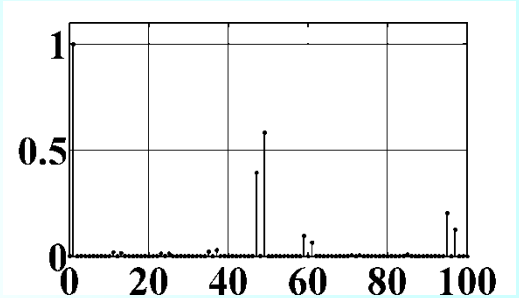
Phase voltage

Pole voltage-high voltage inverter

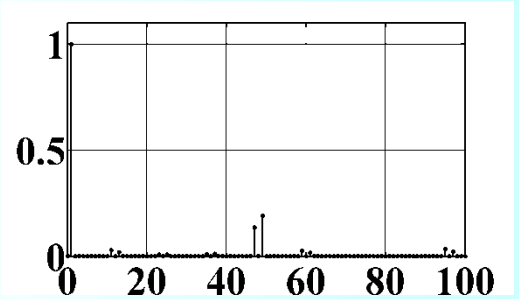
Pole voltage-low voltage inverter

Phase current

Normalized harmonic spectrum of Phase voltage

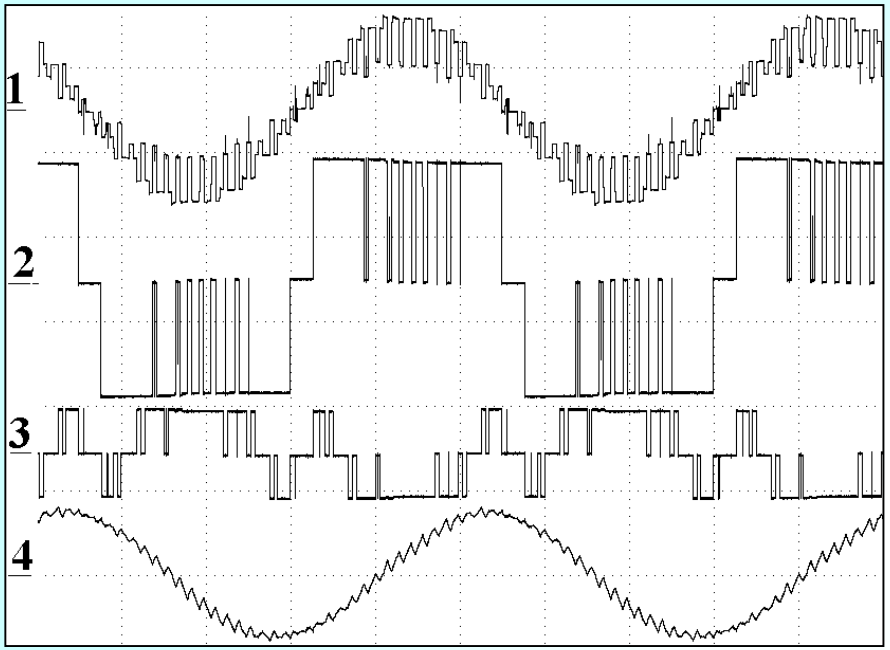


Phase current



- Four samples are taken in each sector and switching takes place entirely in the inner 12-sided polygon.
- The phase voltage harmonics reside at 15x12x4=720 Hz, which is 48 times the fundamental. However, the switching frequency of the pole voltage of INV1 is (24x15=) 360Hz, while that of INV2 is (32x15=) 480Hz.
- The higher voltage inverter switches about 50% of the cycle.

Experimental results-40 Hz operation



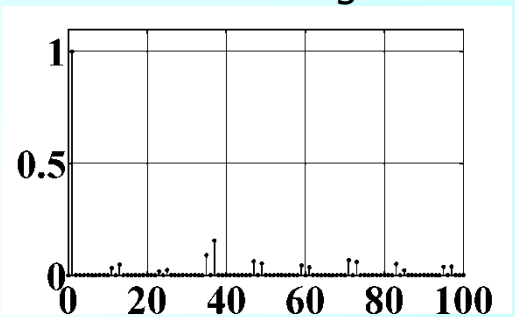
Phase voltage

Pole voltage-high voltage inverter

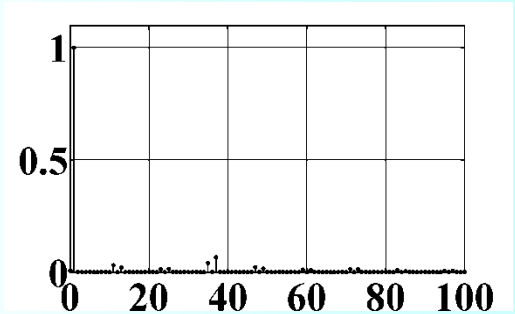
Pole voltage-low voltage inverter

Phase current

Normalized harmonic spectrum of Phase voltage

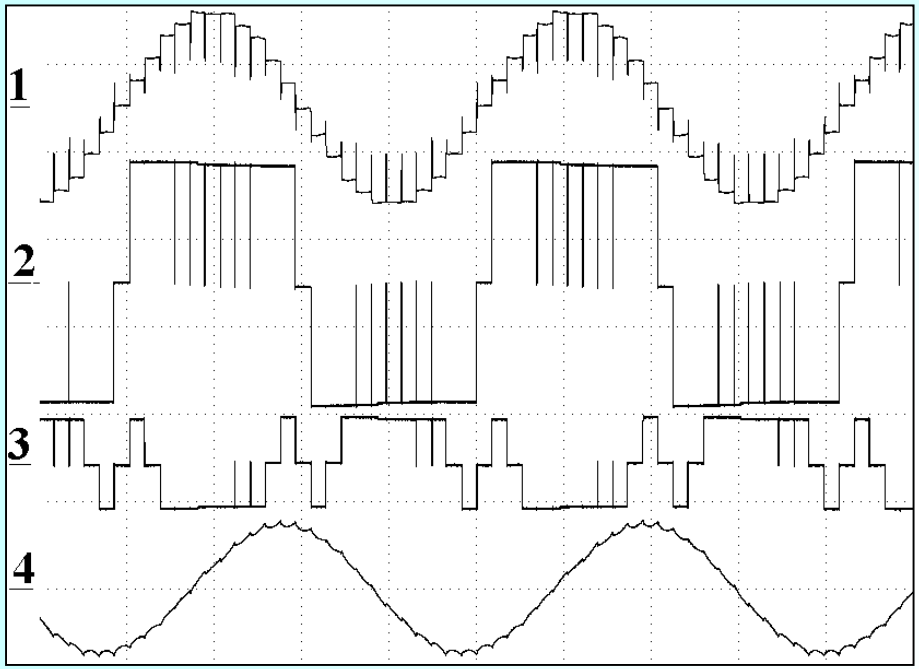


Phase current



- Two samples are taken in each sector and switching takes place between the inner and outer dodecagons.
- This is also seen in the phase voltage waveform, since the outer envelope of the waveform at lower frequency becomes the inner envelope at higher frequency.
- The harmonic spectrum of the phase voltage and current shows the absence of peaky harmonics throughout the range.

Experimental results-48 Hz operation



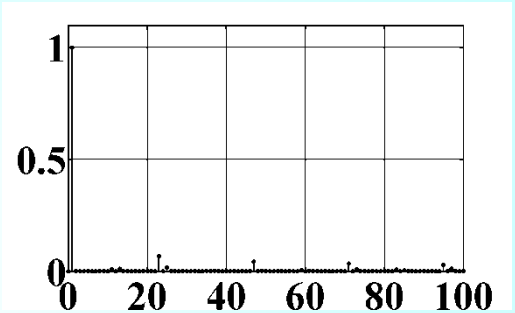
Phase voltage

Pole voltage-high voltage inverter

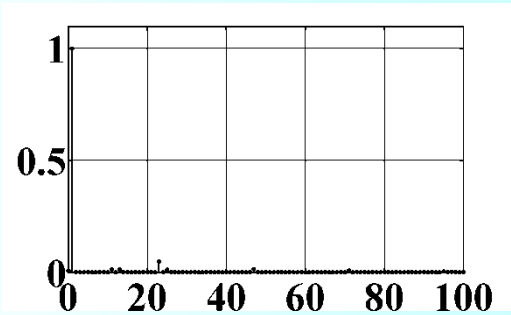
Pole voltage-low voltage inverter

Phase current

Normalized harmonic spectrum of Phase voltage

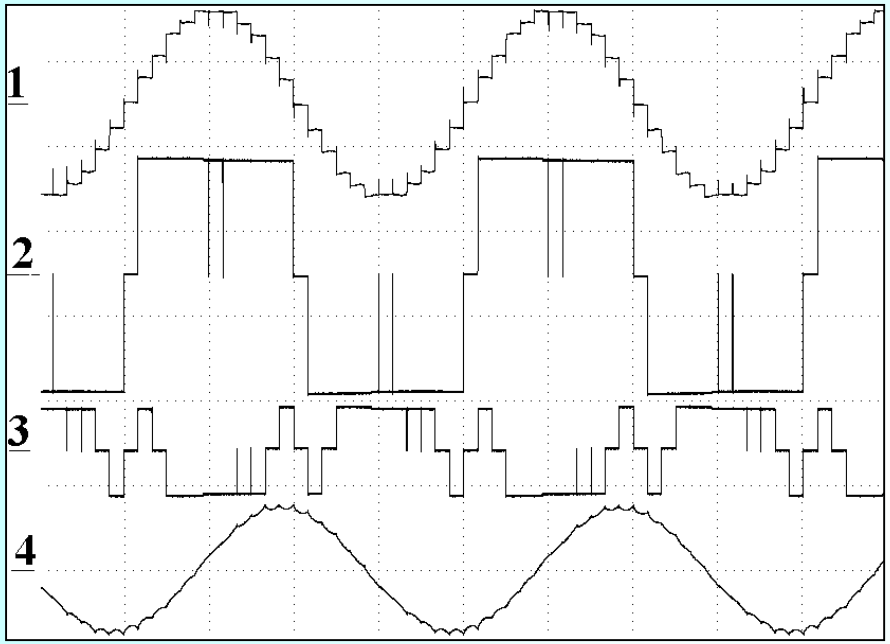


Phase current



- This is the end of the linear modulation of operation.
- Here the number of samples per sector is two, as such the switching frequency sidebands reside around 24 times the fundamental. The switching frequency of the pole voltages of INV1 and INV2 is respectively (48x12=) 576Hz and (48x16=) 768Hz, with an output phase voltage switching frequency of 1152Hz (48x12x2).

Experimental results-49.9 Hz operation



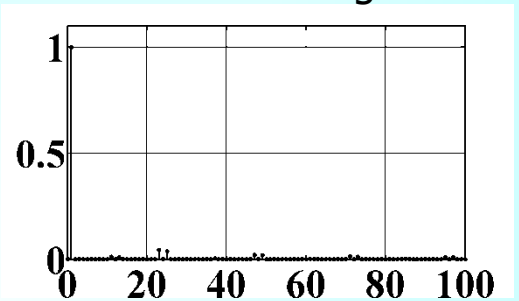
Phase voltage

Pole voltage-high voltage inverter

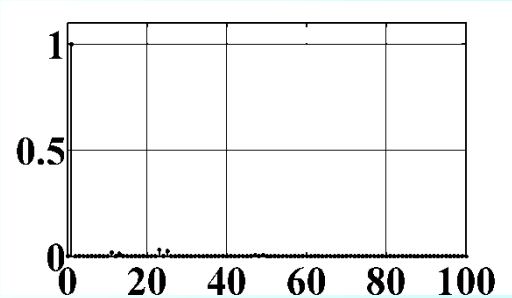
Pole voltage-low voltage inverter

Phase current

Normalized harmonic spectrum of Phase voltage

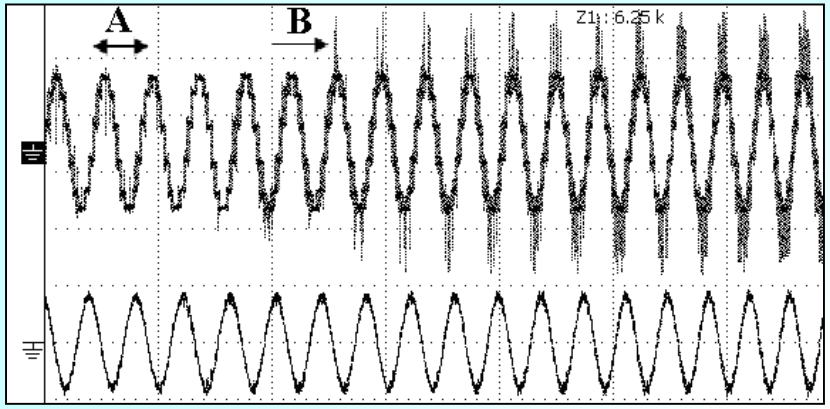


Phase current



•At the end of end over-modulation region, 24 samples are taken in a sector, corresponding to the vertices of the polygon. The figure shows 24 steps in the phase voltage.

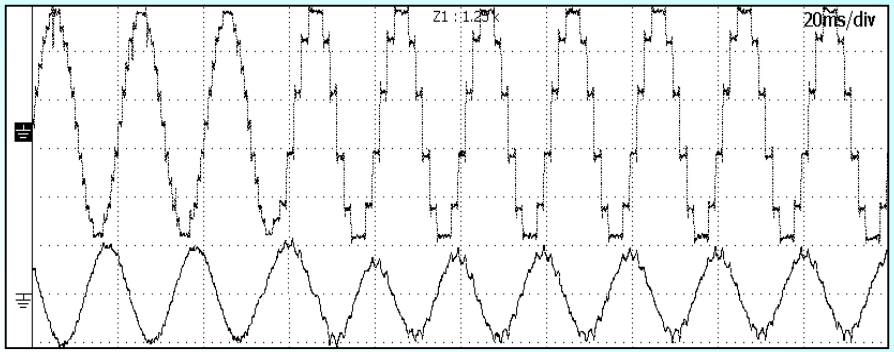
Acceleration of the motor



Transition of motor phase voltage and current from inner to outer 12-sided polygon

Phase voltage

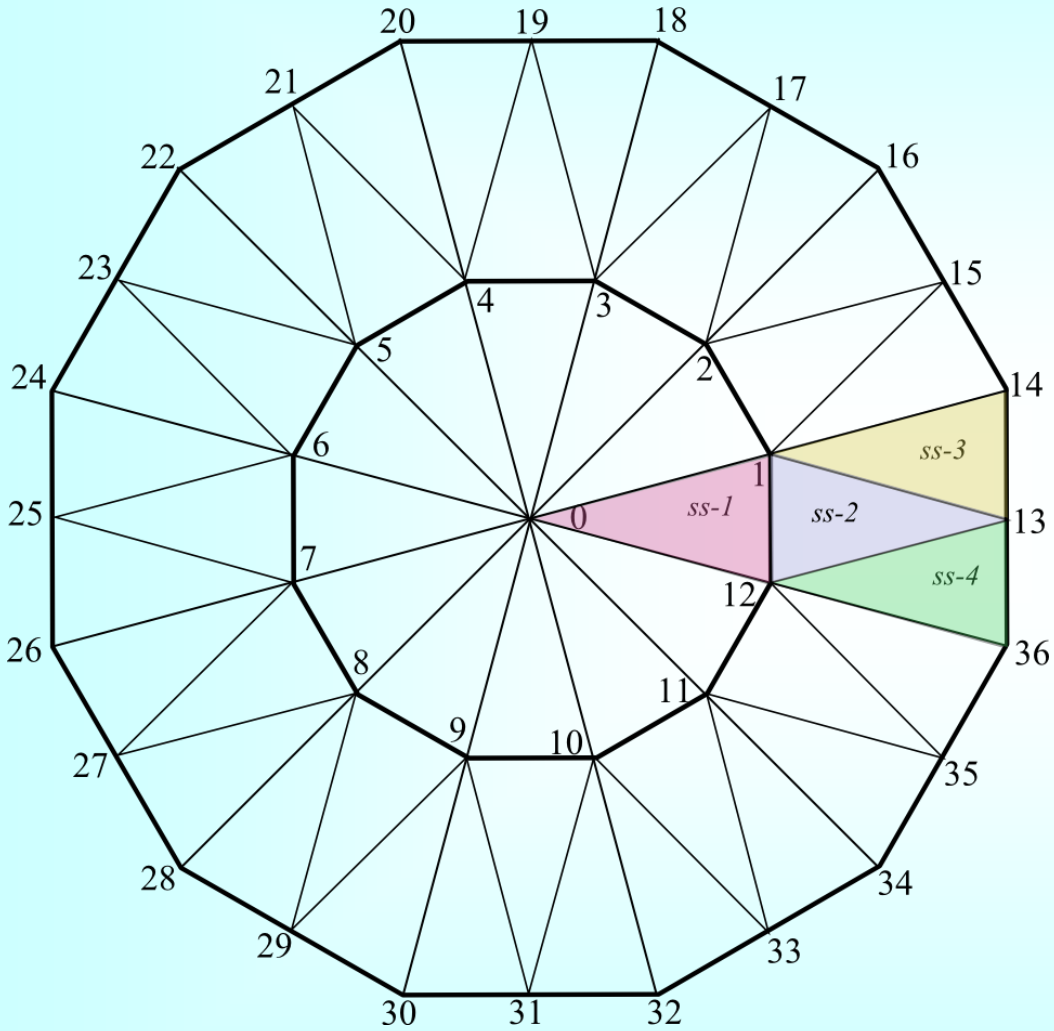
Phase current



Transition of motor phase voltage and current from over-modulation to 12-step operation.

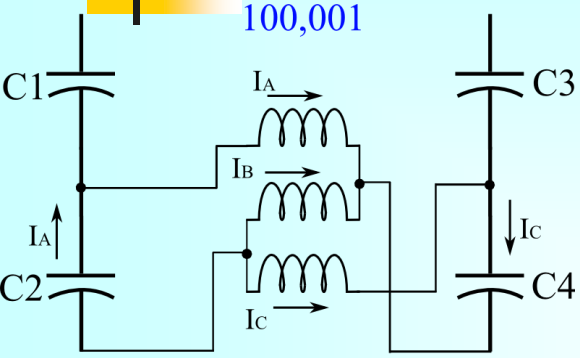
- In both the cases, the motor current changes smoothly as the motor accelerates. This happens because of the use synchronized PWM and total elimination of 6n±1 harmonics, n=odd, from the phase voltage throughout the modulation index.

Capacitor balancing scheme

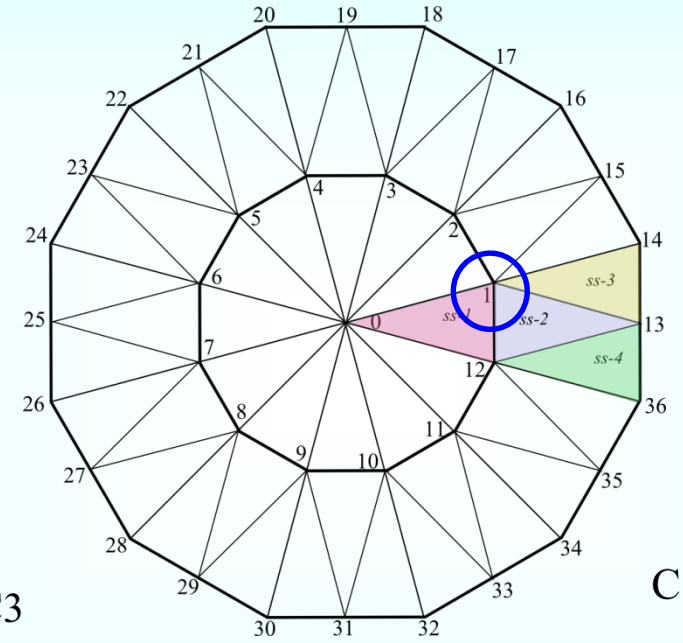


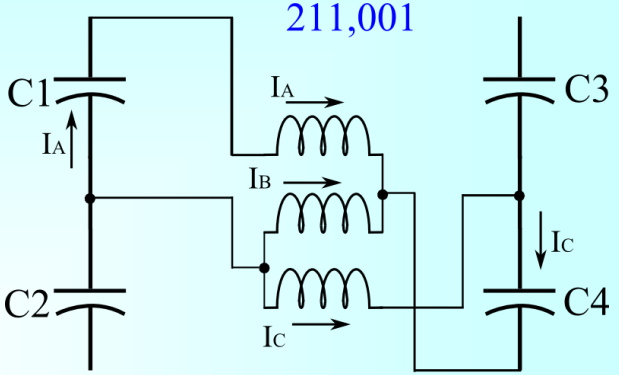
- The inner 12-sided polygonal space vector locations (points 1-12) have four multiplicities which are complementary in nature in terms of capacitor balancing.
- The outer 12-sided polygonal space vector locations (points 13-36) either do not cause any capacitor unbalancing, or have complementary states to maintain capacitor balancing.

Inner 12-sided polygon-switching multiplicities for point-1



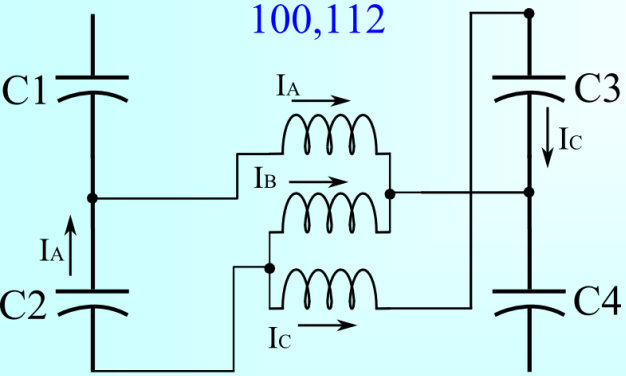
C2 is discharged, C4 is charged.



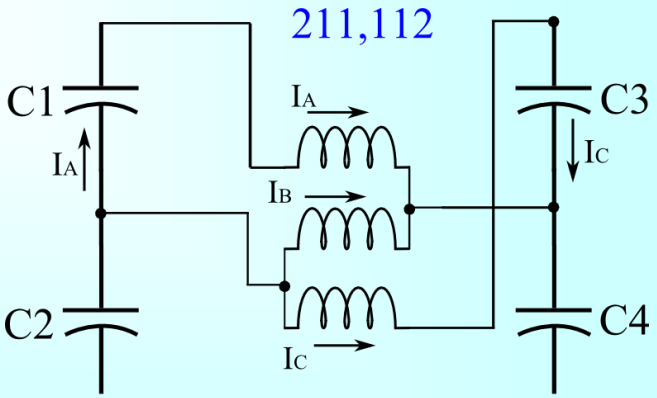


C1 is discharged, C4 is charged.

C2 is discharged, C3 is charged.

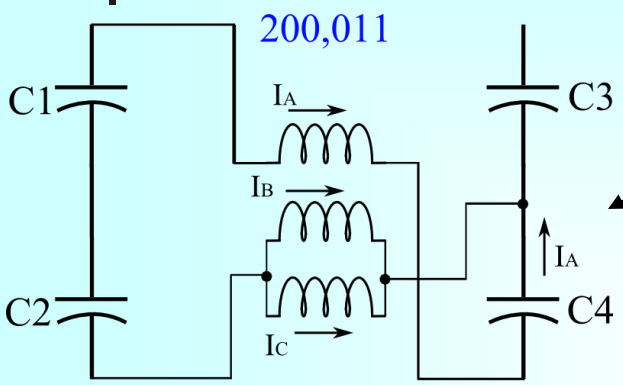


C1 is discharged, C3 is charged.



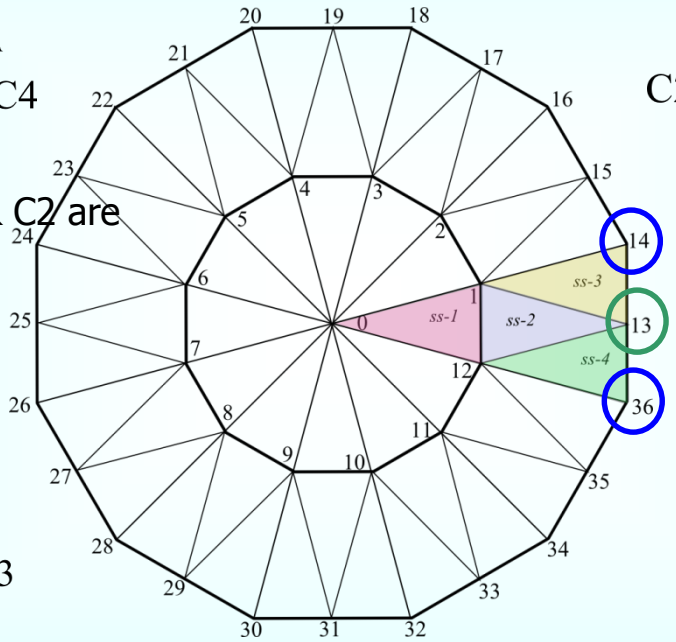
The four switching multiplicities are complementary in nature in terms of capacitor balancing.

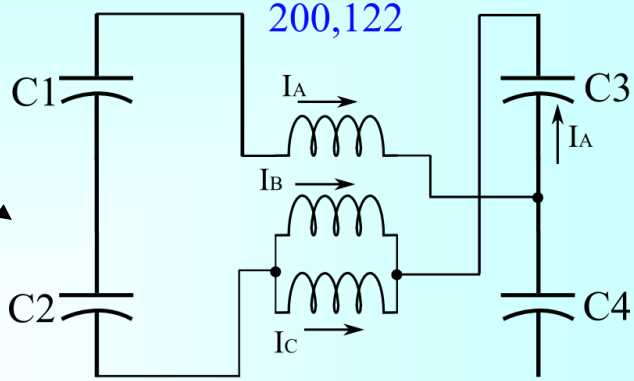
Outer 12-sided polygon-switching multiplicities



C4 is discharged, C1 & C2 are undisturbed.

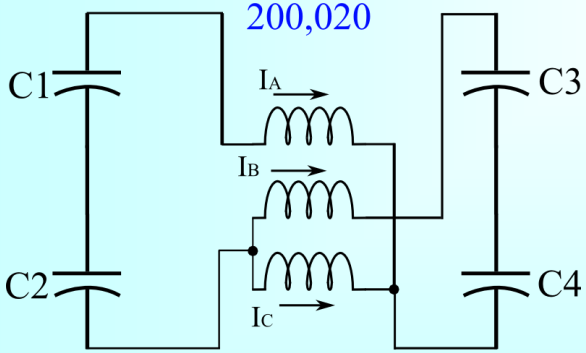
Point-13, two multiplicities



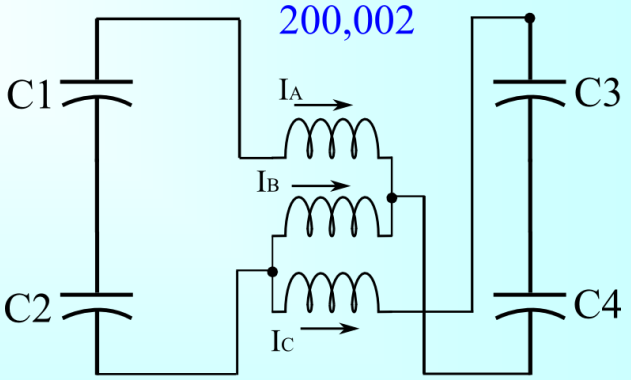


C3 is discharged, C1 & C2 a undisturbed.

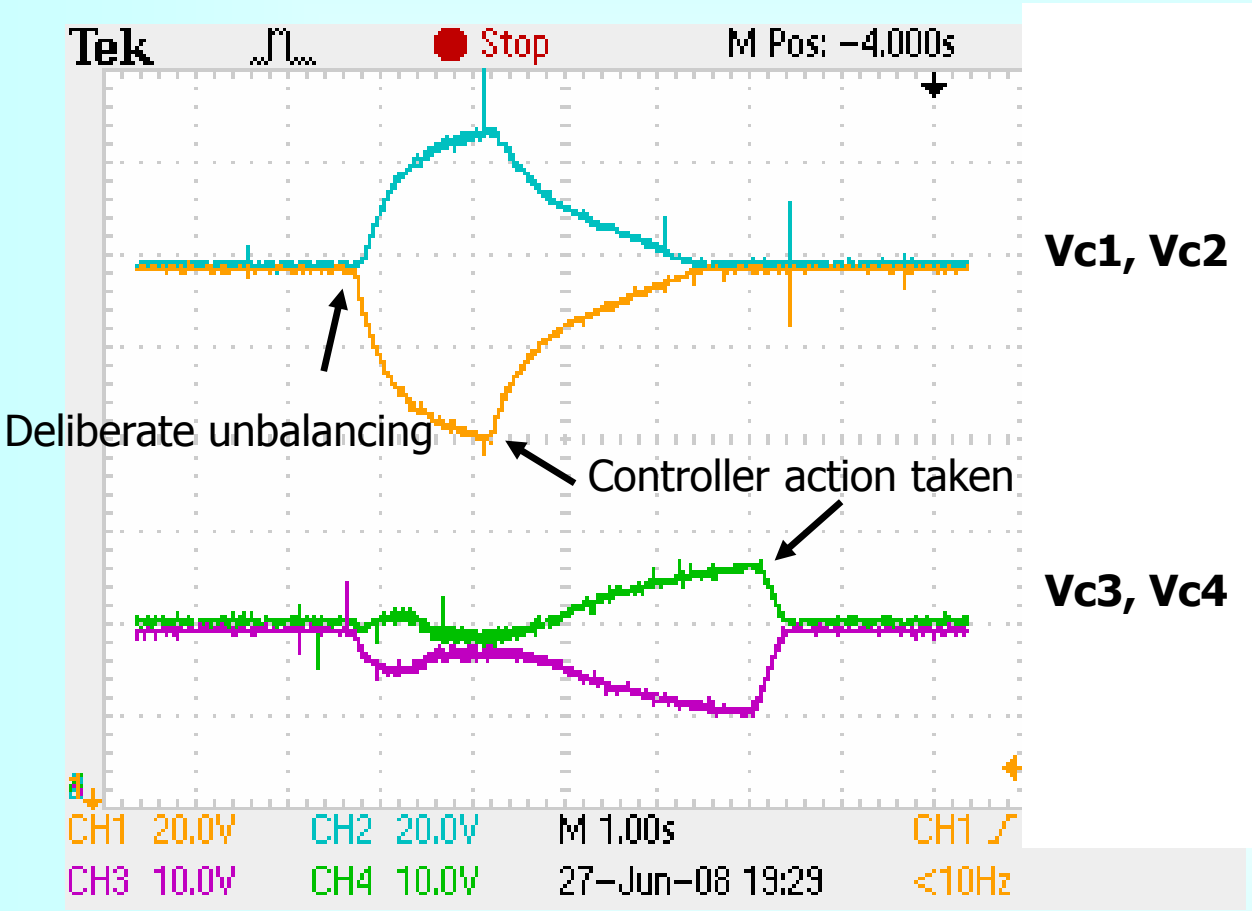
Point-36: no multiplicity, no capacitor disturbance



Point-14: no multiplicity, no capacitor disturbance



Experimental Results-capacitor unbalancing at 20 Hz

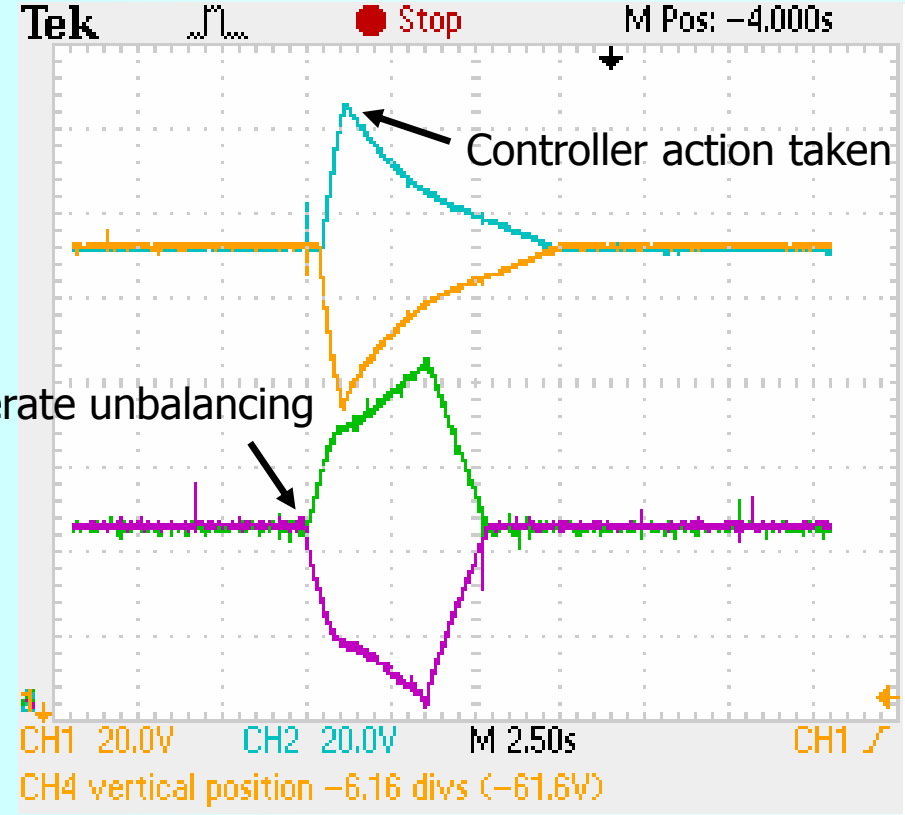


- Capacitor unbalance is done at steady state with the motor running at 20 Hz speed.
- Both side capacitors are deliberately unbalanced and after some time controller action is taken.

C1,C2 : higher voltage side capacitors

C3,C4 : lower voltage side capacitors

Experimental Results-capacitor unbalancing at 40Hz



Vc1, Vc2

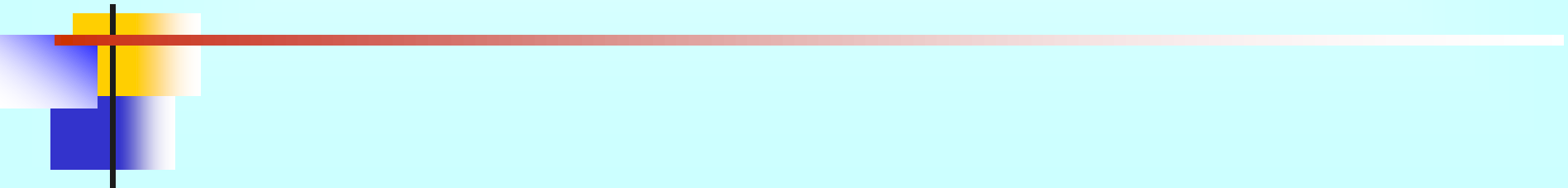
Vc3, Vc4

- Both the sides are made unbalanced at the same time and are seen to come back to the balanced state.
- Compared to the 20 Hz case, it requires more time to restore voltage balance, since the number of multiplicities in the outer polygon is less.

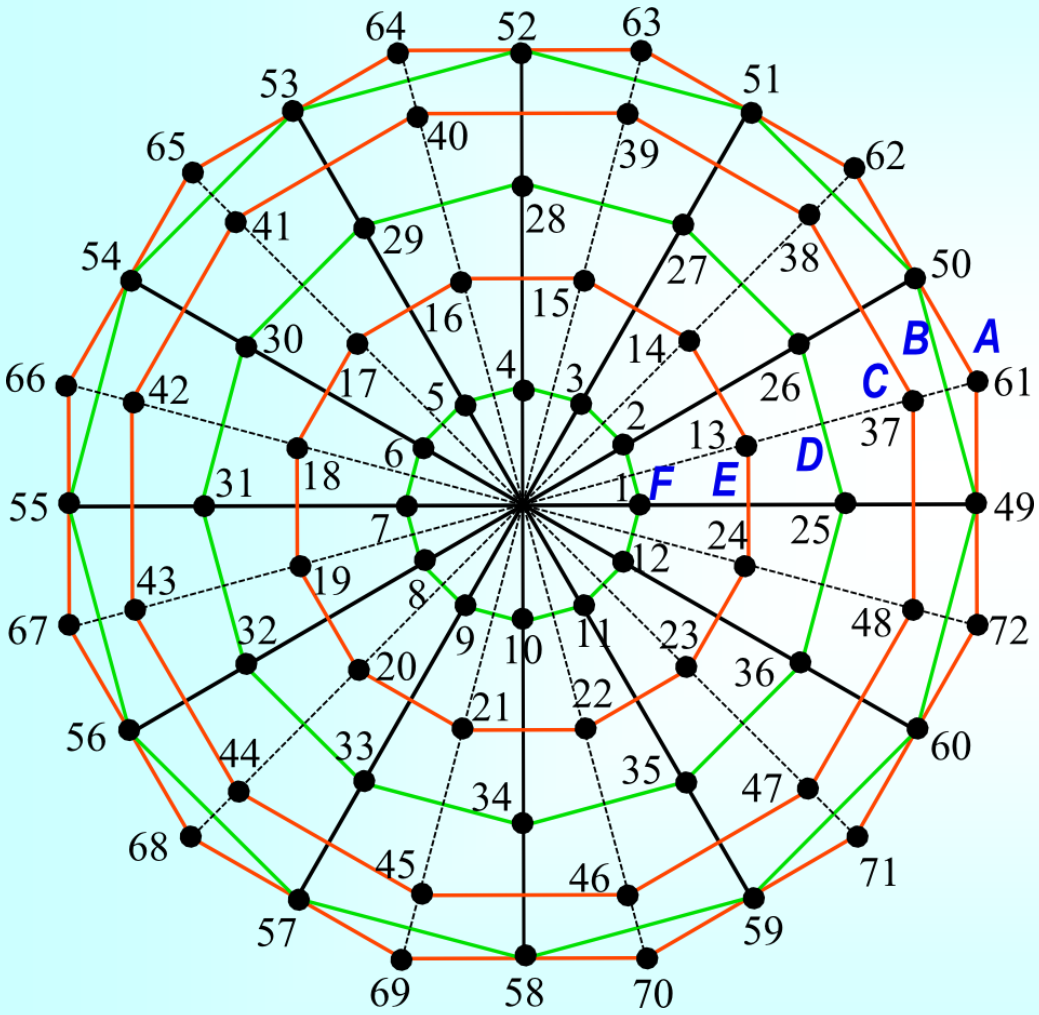
C1,C2 : higher voltage side capacitors

C3,C4 : lower voltage side capacitors

Part-III
A Voltage Space Vector Diagram Formed By Six Concentric Dodecagons



Space Vector Structure



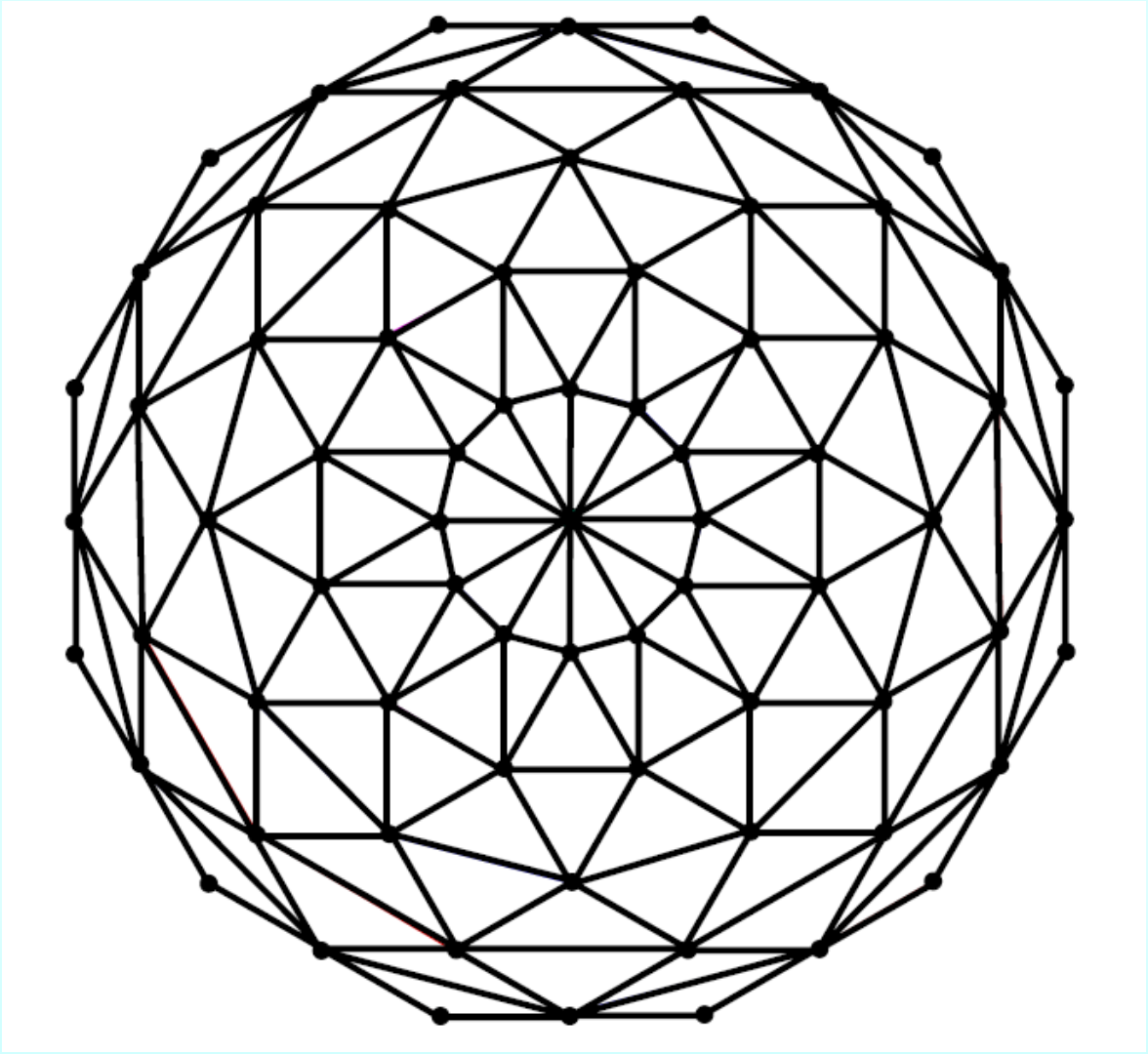
- The space vector structure consists of six concentric dodecagonal structures - A, B, C, D, E and F.

- These are grouped as type-1 and type-2 dodecagons, where type-2 dodecagons (A, C and E) lead type-1 dodecagons (B, D and F) by 15^0.

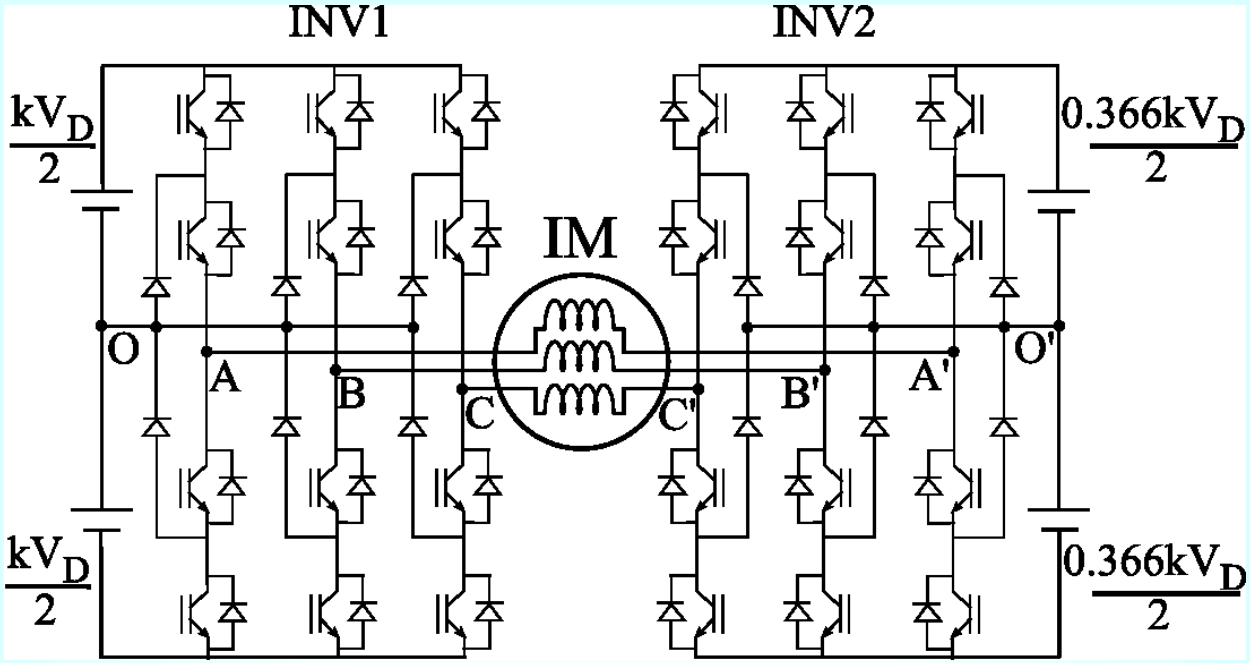
- The radii of these polygons are in the ratio *r1*: *r2*: *r3*: *r4*: *r5*: *r6* = 1: *cos* $(\pi/12)$: *cos* $(2\pi/12)$: *cos* $(3\pi/12)$: *cos* $(4\pi/12)$: *cos* $(5\pi/12)$.

- The entire space vector structure is divided into 12 sectors each of width 30^0.

Sub division of the voltage space vector region with sub sectors



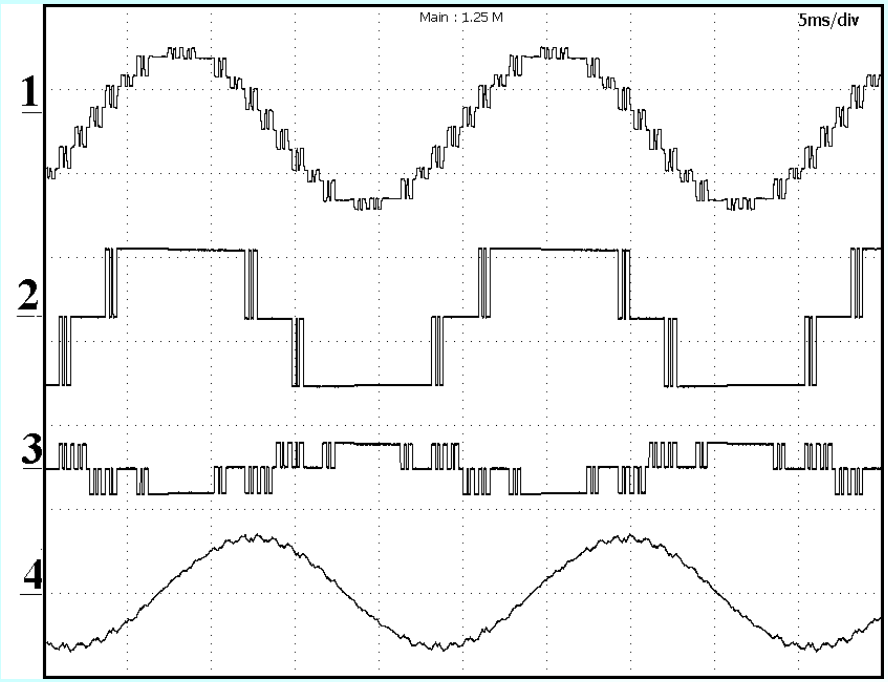
Power Circuit of the Inverter



• The power circuit of the inverter consists of 2 three level NPC inverters feeding an open end induction motor.

•These two inverters are fed from isolated dc voltage sources having voltage ratio of 1:0.366. This ratio of voltages is obtained from a combination of star delta transformers since 1:0.366= (√3+1):1.

Experimental results-46 Hz operation



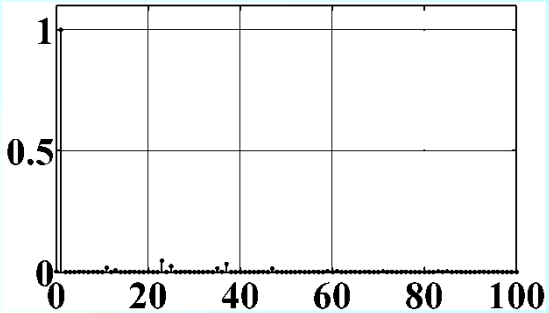
Phase voltage

Pole voltage- high voltage inverter

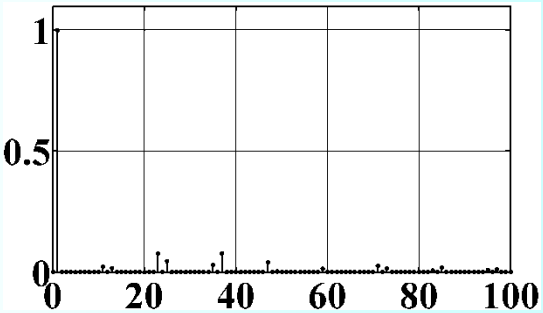
Pole voltage-low voltage inverter

Phase current

Normalized harmonic spectrum of Phase voltage

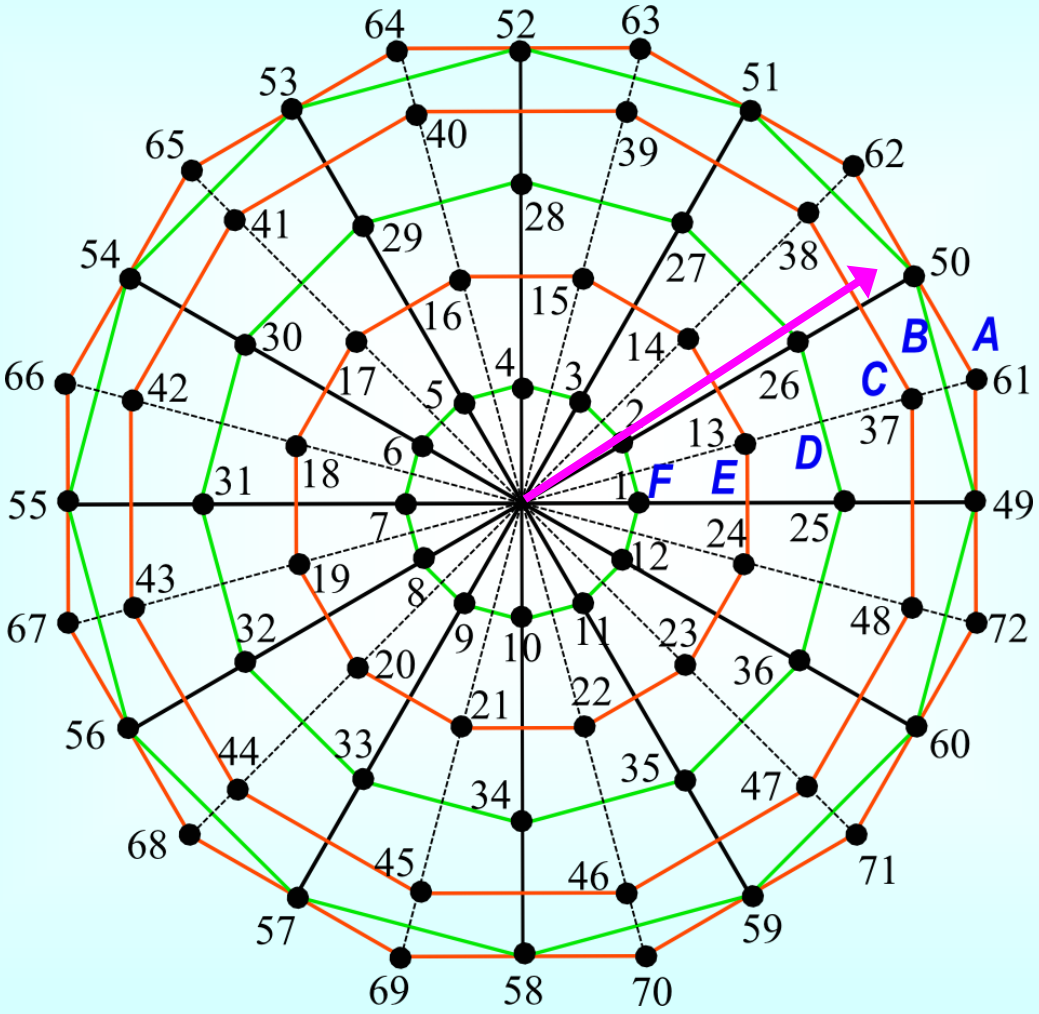


Phase current

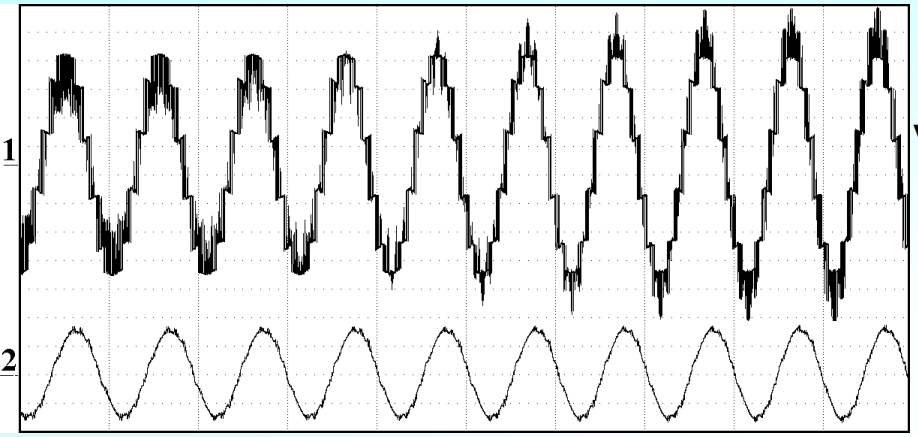


- The phase voltage waveform of phase A distinctly shows the presence of 18 steps in a cycle.
- The phase voltage harmonics reside at (24x45=) 1080 Hz, while individual devices of INV1 and INV2 switch at (5x45=) 225 Hz and (15x 45=) 675 Hz respectively.

Operation at 46 Hz



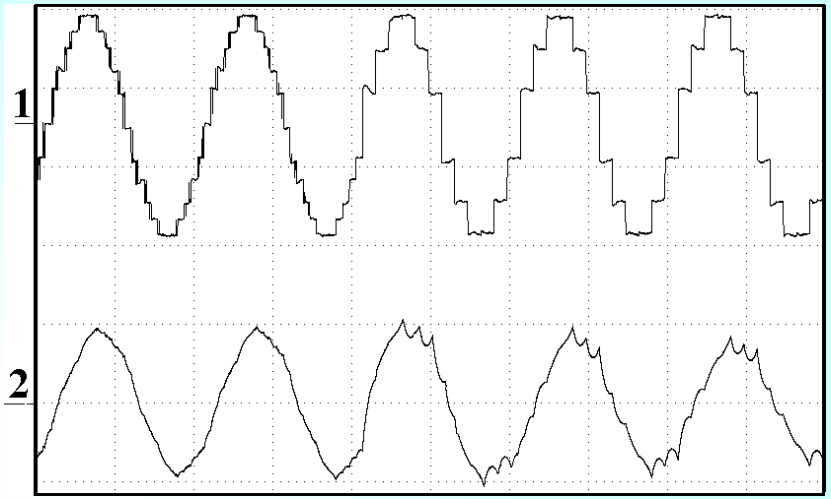
Motor acceleration with open loop V/f Control



Transition of motor phase voltage and current from 20 Hz to 30Hz

Phase voltage

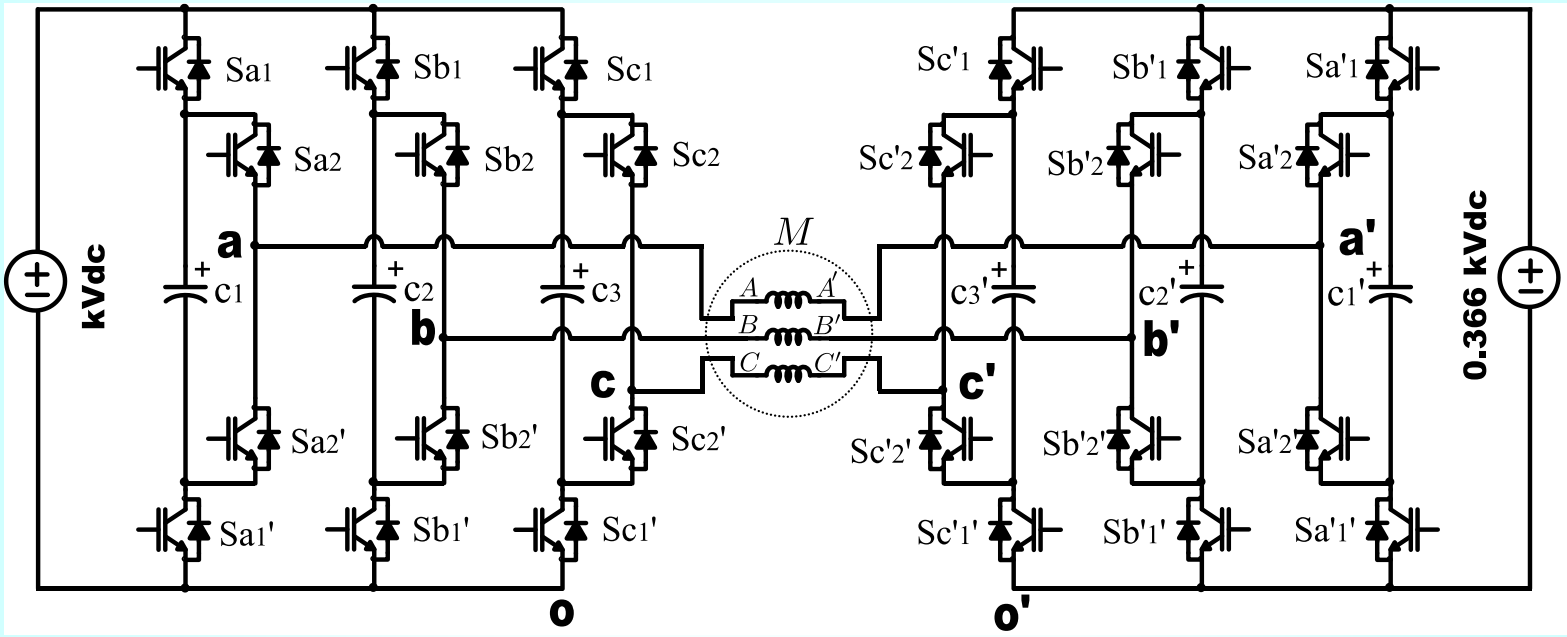
Phase current



Transition of motor phase voltage and current from over-modulation to 12-step operation.

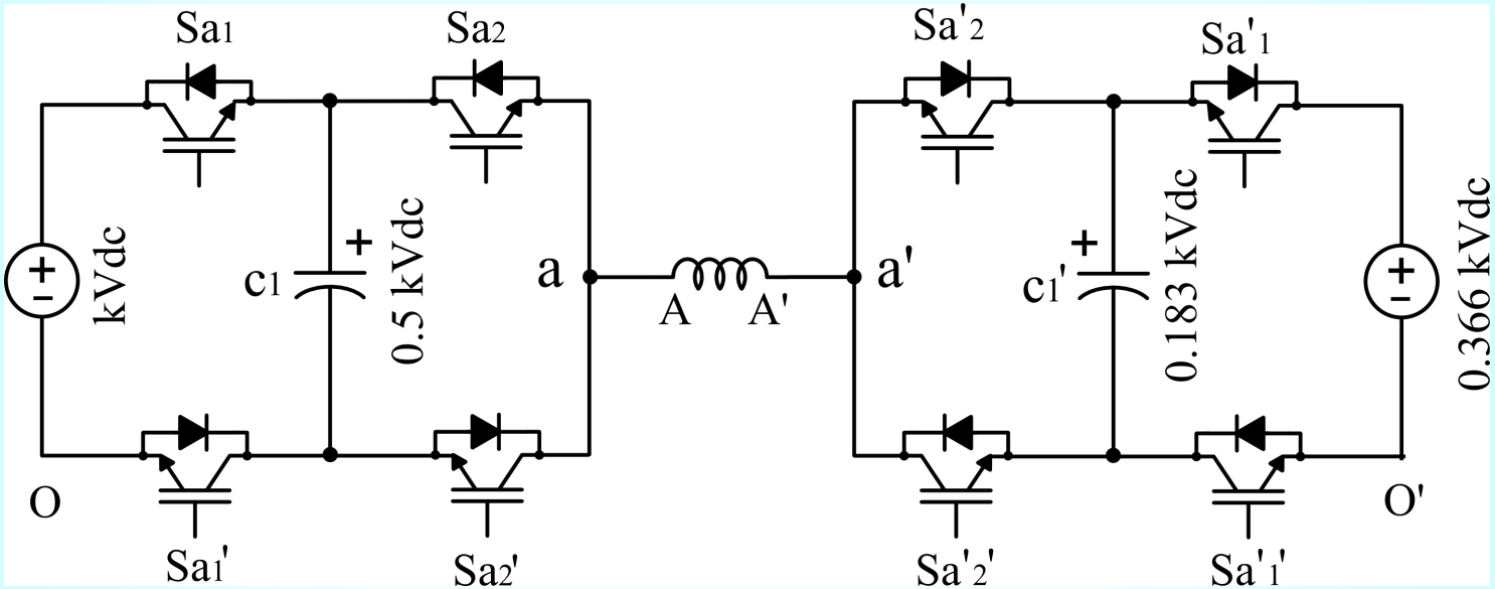
- In the first case, the reference vector starts from inside dodecagon E, crosses through the boundary of it and finally settles below the D dodecagon.
- In the second case, the number of samples per sector is changed from 2 to 1 at 12-step operation.
- Correct calculation of the PWM timings and complete elimination of the 5^{th} and 7^{th} order harmonics ensure that the motor current changes smoothly during the transition.

Proposed Topology

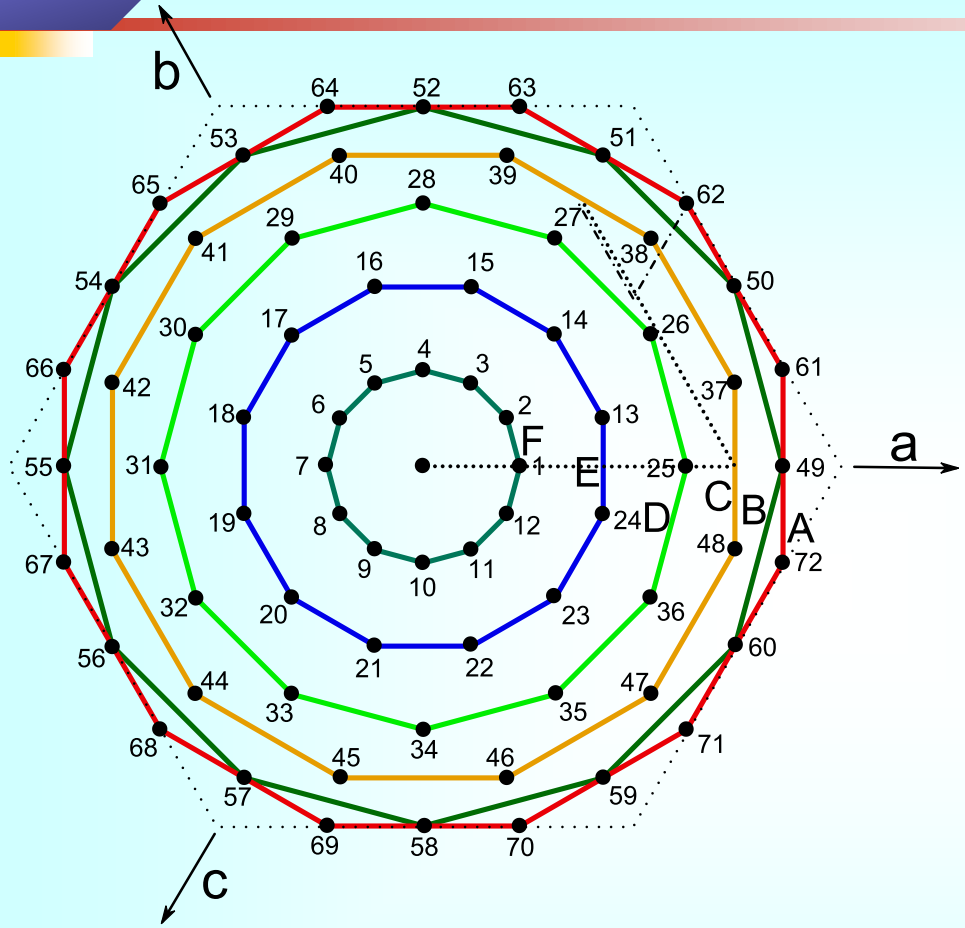


Phase winding connections

Phase-A winding connections



Space vector Diagram



The space vector is:

$$V_R = (V_{ao} - V_{a'o}) + (V_{bo} - V_{b'o'})e^{j120} + (V_{co} - V_{c'o'})e^{j240}$$

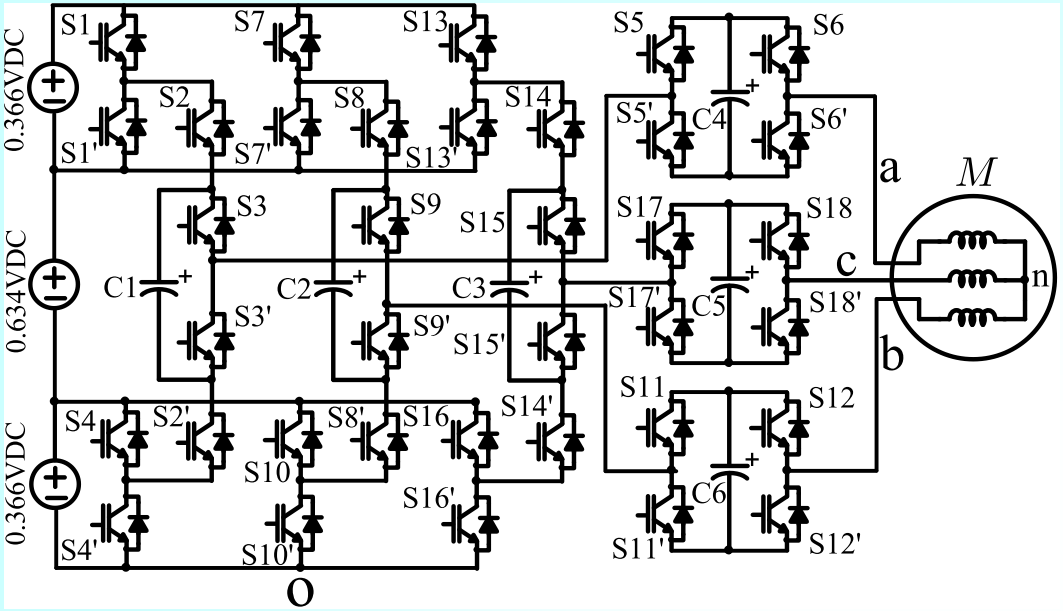
Eg.

point	Vao	Vbo	Vco	Va'o'	Vb'o'	Vc'o'	VR
62	1	1	0	0	0.366	0.366	1.225 kVdc

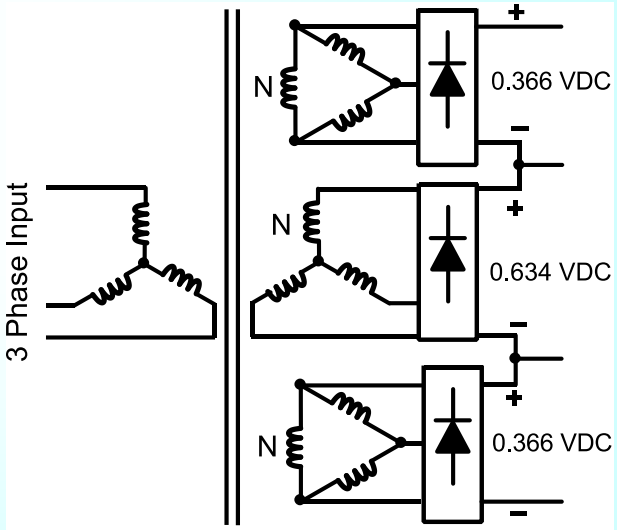
- The total number of space vector combinations is 729 (9^3).
- Only those space vectors are chosen whose tips lie on the vertices of twelve sided polygons (dodecagons).
- The maximum radius of the dodecagonal space vector diagram is 1.225 KVdc.
- 1.225 kVdc=0.9665 Vdc, or k=0.789

Name of Dodecagon	Radius
A	1.225 kVdc
B	1.183 kVdc
C	1.061 kVdc
D	0.866 kVdc
E	0.612 kVdc
F	0.317 kVdc

A hybrid multilevel inverter system based on dodecagonal space vectors for medium voltage IM drives



Power stage



Transformer connection scheme used

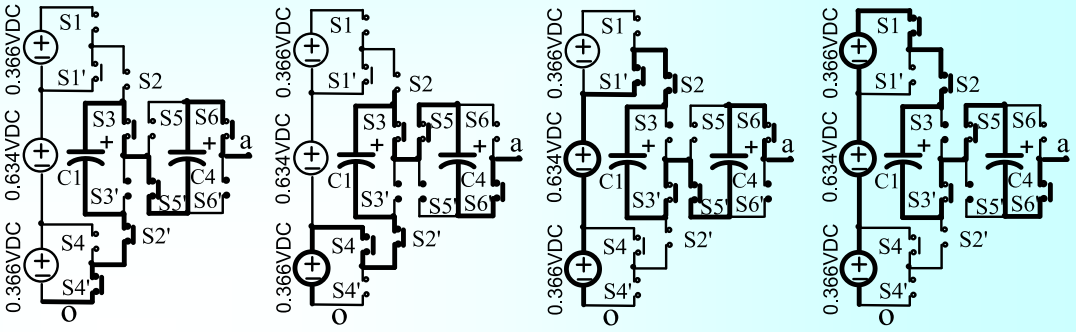
Phase-A winding connections and pole voltage levels

Table 1: Different ways to generate Phase-A Pole Voltages and he effect on capacitor voltages

Pole Voltage Levels	Method of generation	Effect on capacitors when current is positive (towards the motor terminal)	
		C1	C4
0.183VDC	Vc4	No effect	Discharging
	0.366VDC-Vc4	No effect	Charging
0.366VDC	0.366VDC	No effect	No effect
0.5VDC	Vc1	Discharging	No effect
	VDC-Vc1	Charging	No effect
0.683VDC	Vc1+Vc4	Discharging	Discharging
	0.366VDC+Vc1-Vc4	Discharging	Charging
	VDC-Vc1+Vc4	Charging	Discharging
	1.366VDC-Vc1-Vc4	Charging	Charging
0.866VDC	0.366+Vc1	Discharging	No effect
	1.366VDC-Vc1	Charging	No effect
1VDC	VDC	No effect	No effect
1.183VDC	VDC+Vc4	No effect	Discharging
	1.366VDC-Vc4	No effect	Charging
1.366VDC	1.366VDC	No effect	No effect
0	0	No effect	No effect

Note: Vc1 (0.5VDC) and Vc4 (0.183VDC) are the voltage across the floating capacitors C1 and C4 respectively.

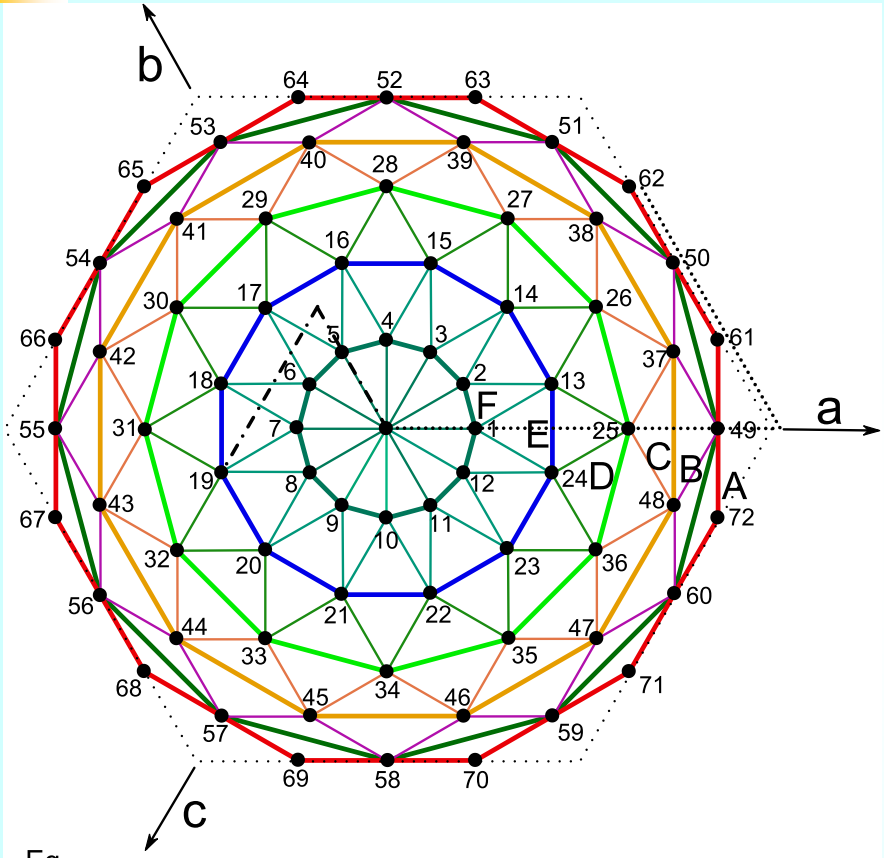
Example:



Different methods of generation of pole voltage levels 0.683VDC (Vc_1=0.5VDC, Vc_4=0.183VDC)

- It is a 9-level (asymmetric-levels) inverter topology
- For controlling the voltage of the capacitors, depending on the current direction, we can switch the devices properly in every sampling period, while ensuring that the required voltage level is always generated by switching-state redundancies.

Space vector Diagram



Eg. point	Vao	Vbo	Vco	V_R
19	0	0.5	0.683	0.612kVdc ∠-165
62	1.366	1	0	1.225kVdc ∠45

The space vector is:

$$V_R = V_{ao} + V_{bo}\,e^{j120} + V_{co}\,e^{j240}$$

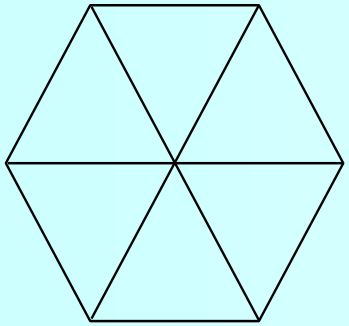
- The total number of space vector combinations is 729 (9^3).
- Only those space vectors are chosen whose tips lie on the vertices of twelve sided polygons (dodecagons).

Name of Dodecagon	Radius
A	1.225 VDC
B	1.183 VDC
C	1.061 VDC
D	0.866 VDC
E	0.612 VDC
F	0.317 VDC

Multilevel Octadecagonal Space Vector Generation for Induction Motor Drives by Cascading Asymmetric Three Level Inverters

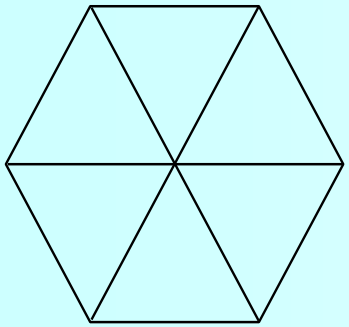
Evolution of space vector structures (Hexagonal,12-sided and 18-sided)

2-level

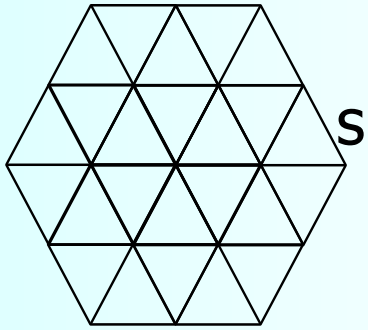


Evolution of space vector structures (Hexagonal,12-sided and 18-sided)

2-level



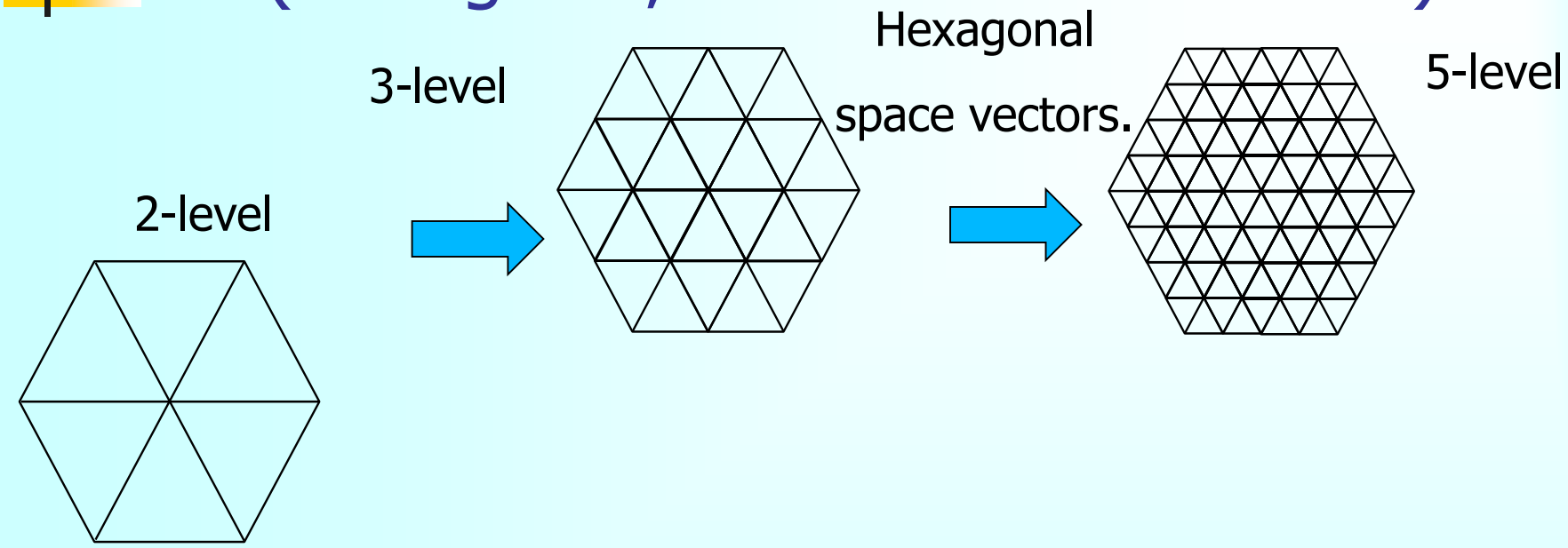
3-level



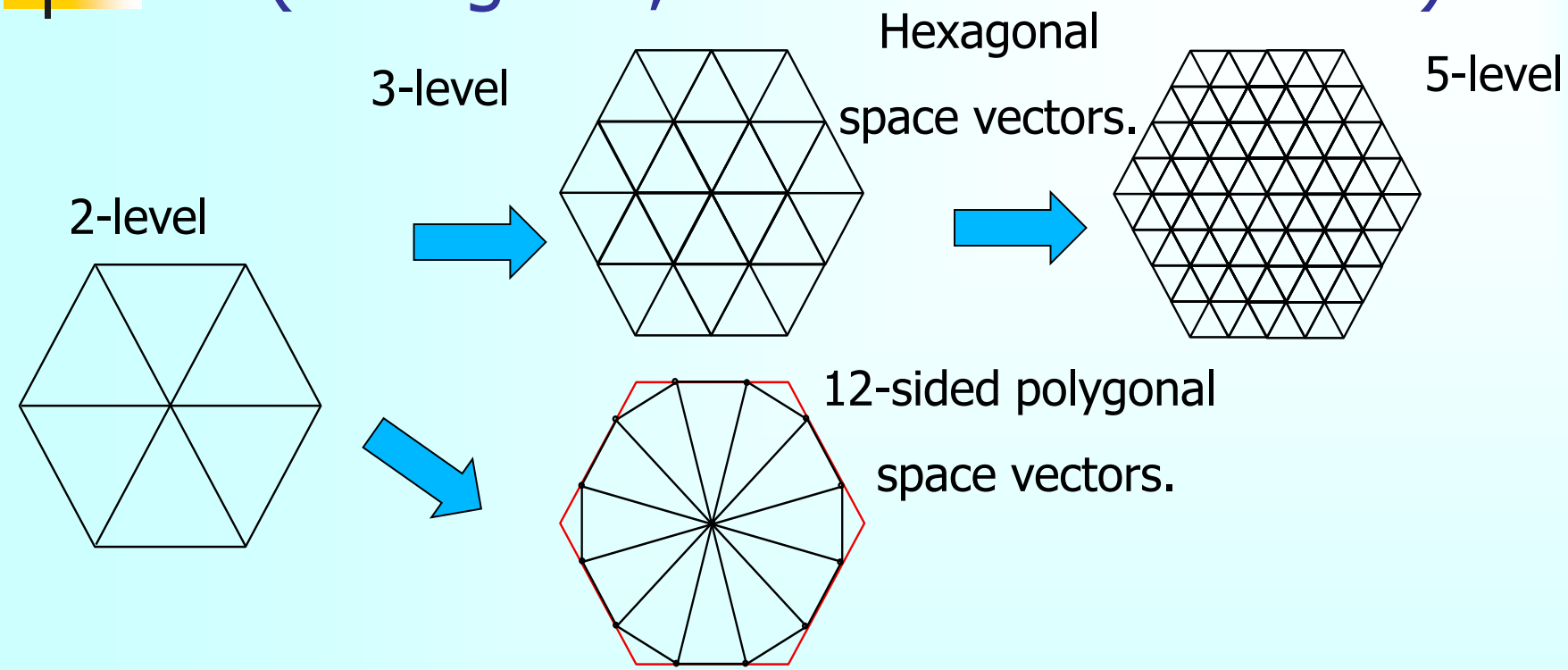
Hexagonal

space vectors.

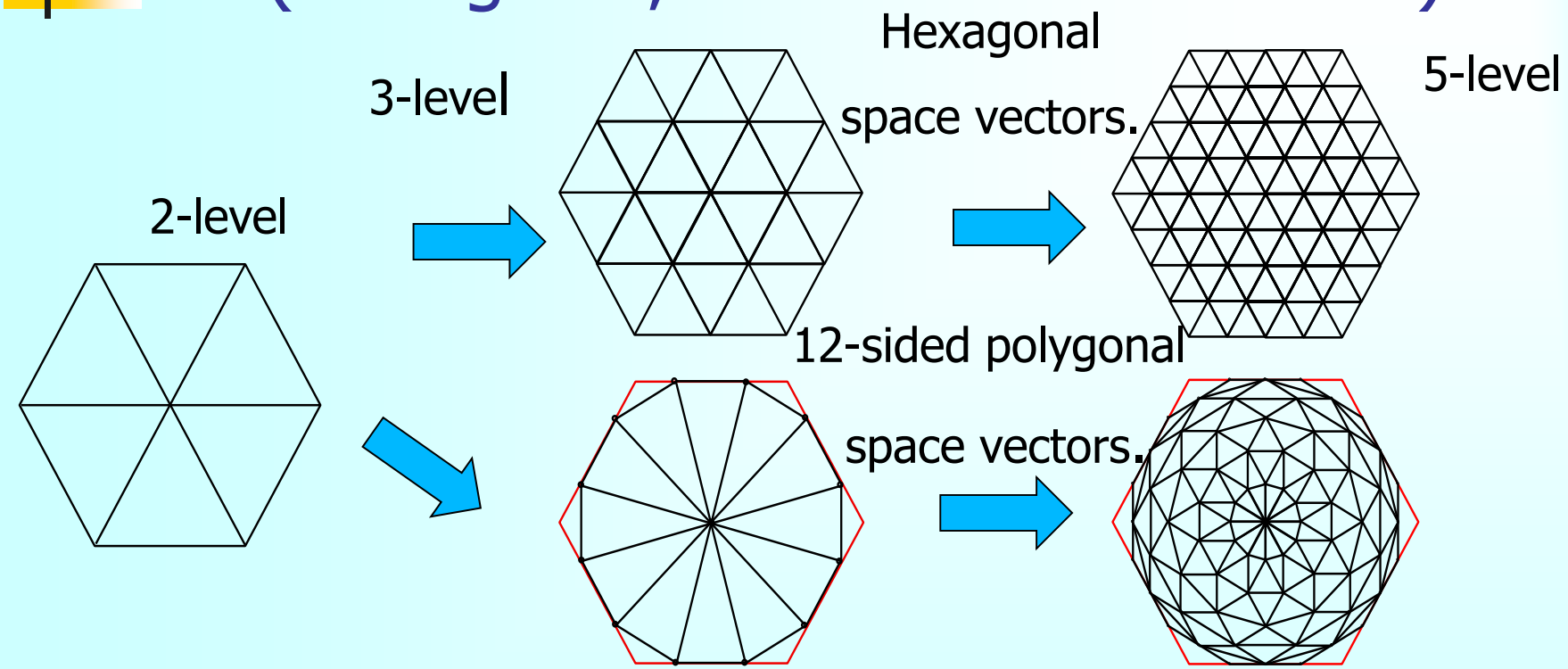
Evolution of space vector structures (Hexagonal,12-sided and 18-sided)



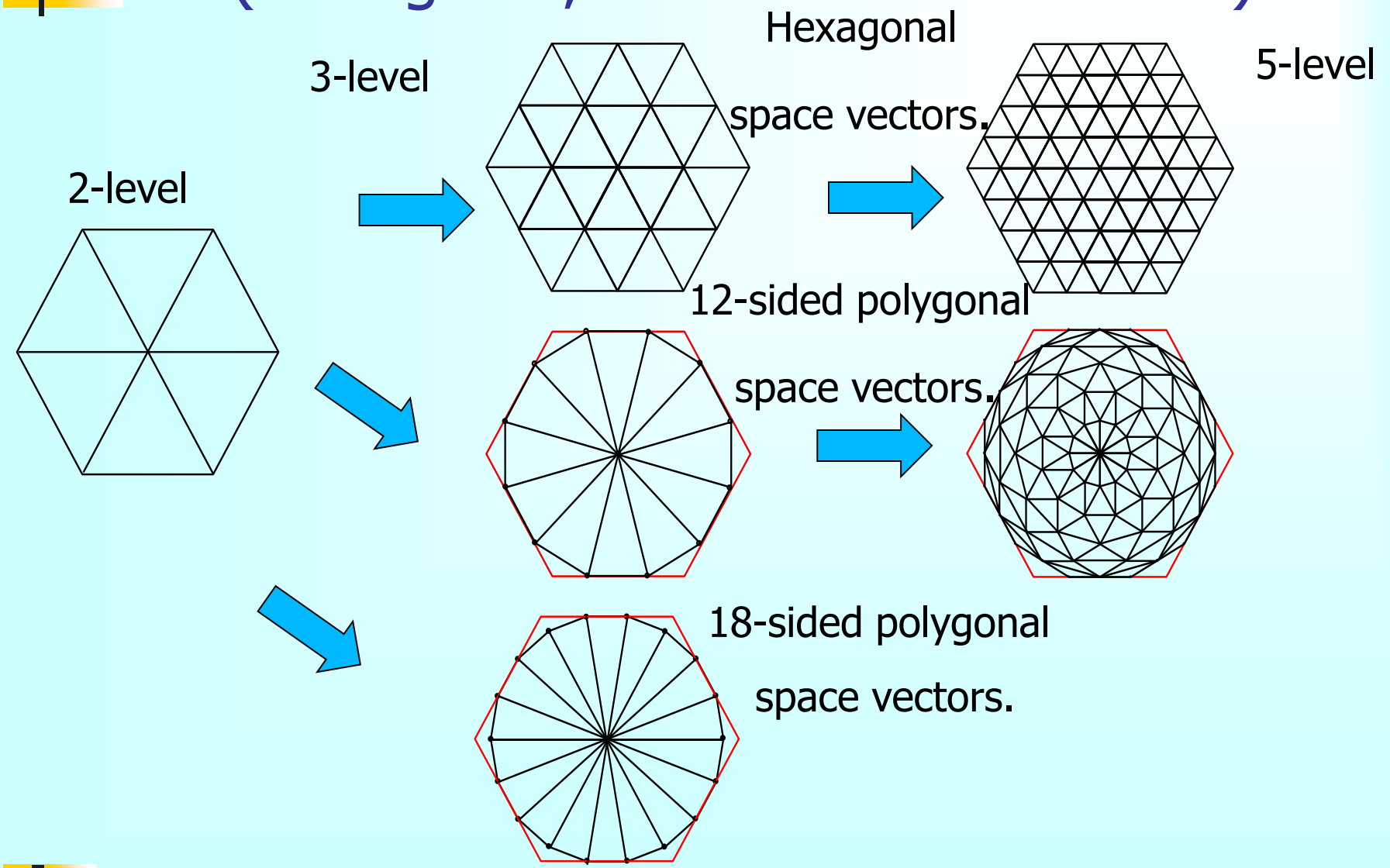
Evolution of spce vector structures (Hexagonal,12-sided and 18-sided)



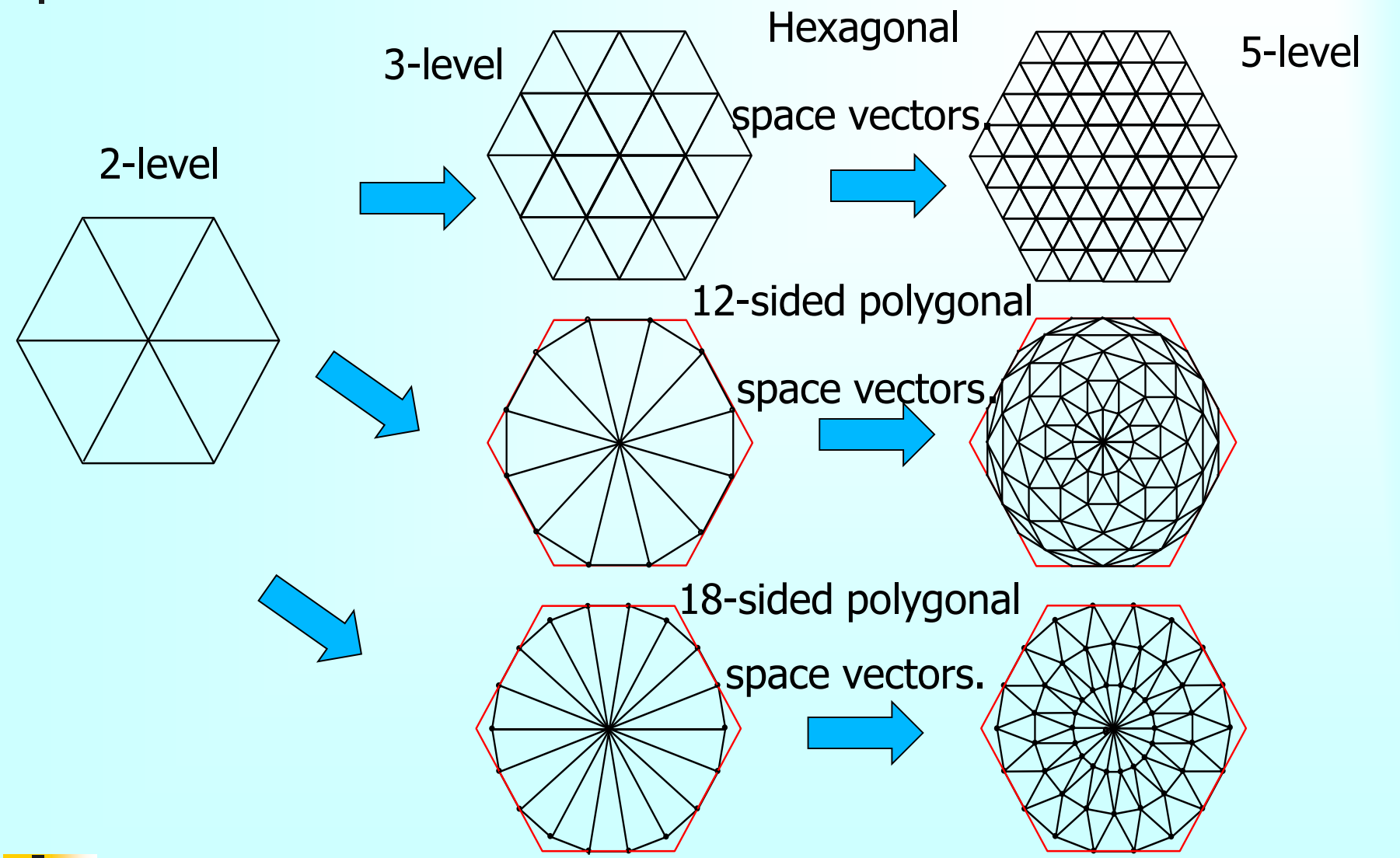
Evolution of space vector structures (Hexagonal,12-sided and 18-sided)



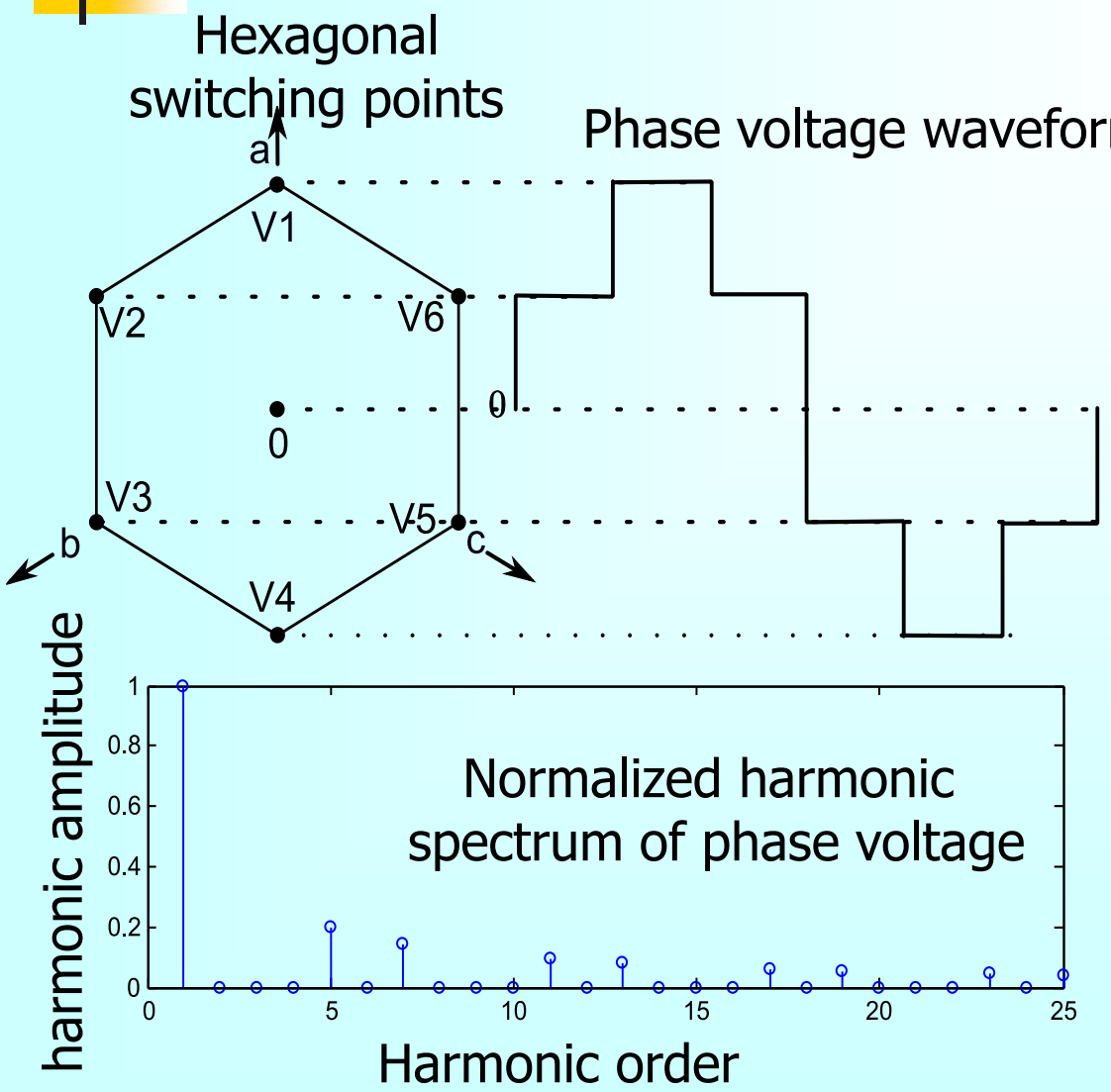
Evolution of space vector structures (Hexagonal,12-sided and 18-sided)



Evolution of space vector structures (Hexagonal,12-sided and 18-sided)



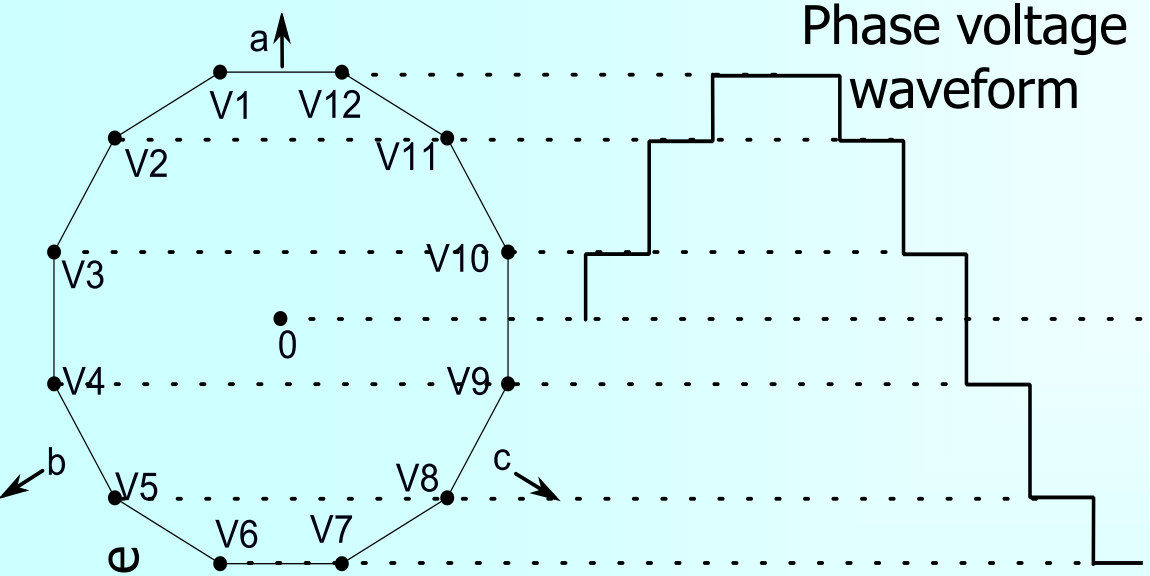
Harmonics for hexagonal switching



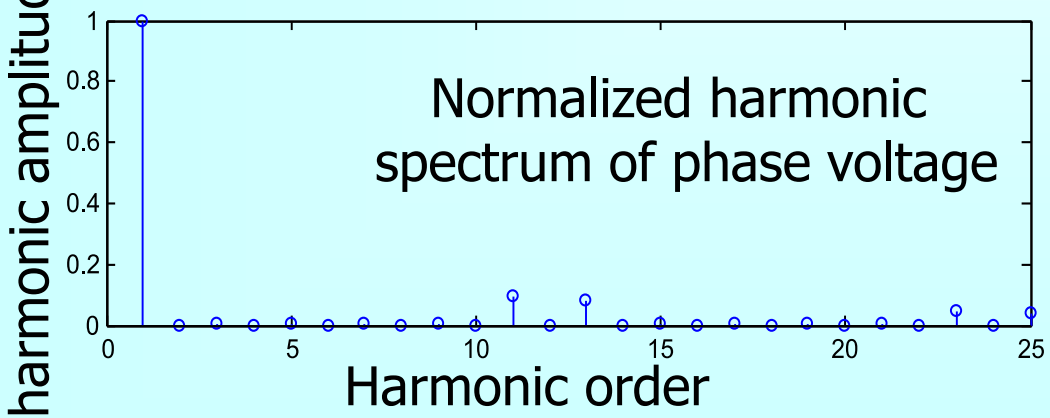
- Harmonics present present for hexagonal switching are 5,7,11,13,17,19, ...

Harmonics for dodecagonal switching

Dodecagonal switching points

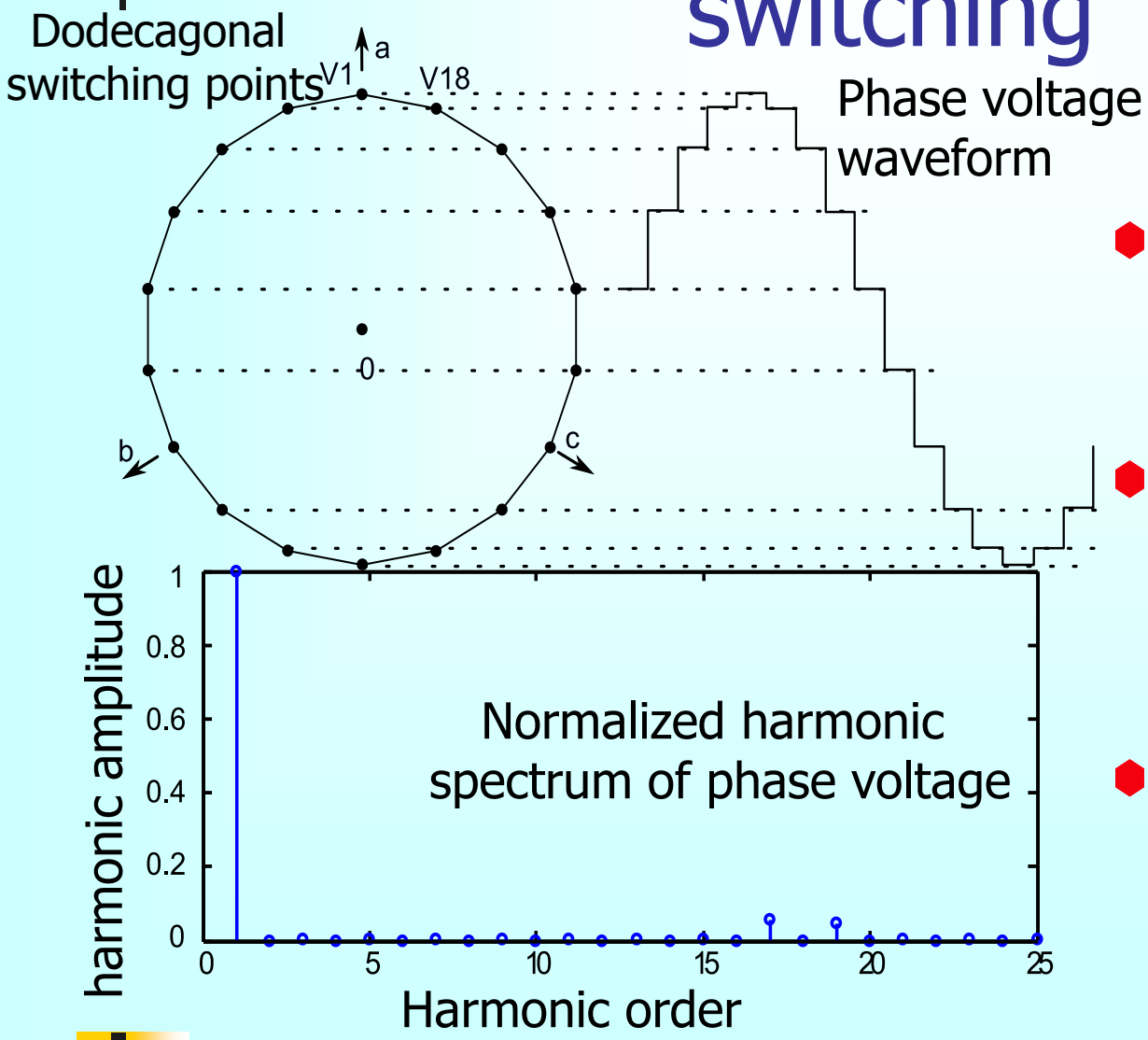


Phase voltage waveform



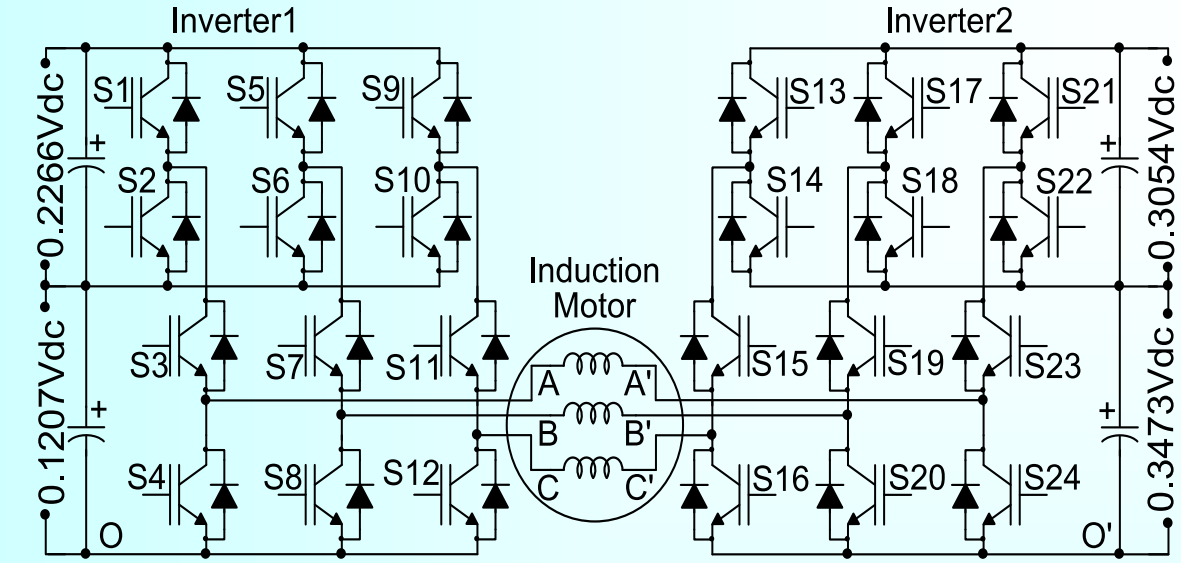
- $(6n\pm1), n=odd$ harmonics are completely absent
- Harmonics present present for dodecagonal switching are 11,13,23,25, ...
- Waveform has less dv/dt and less Harmonic distortion compared to hexagonal switching

Harmonics for octadecagonal switching



- 5th, 7th, 11th, 13th harmonics are completely absent
- Harmonics present present for dodecagonal switching are 17,19,35,37...
- Waveform has less dv/dt and less Harmonic distortion compared with dodecagonal switching

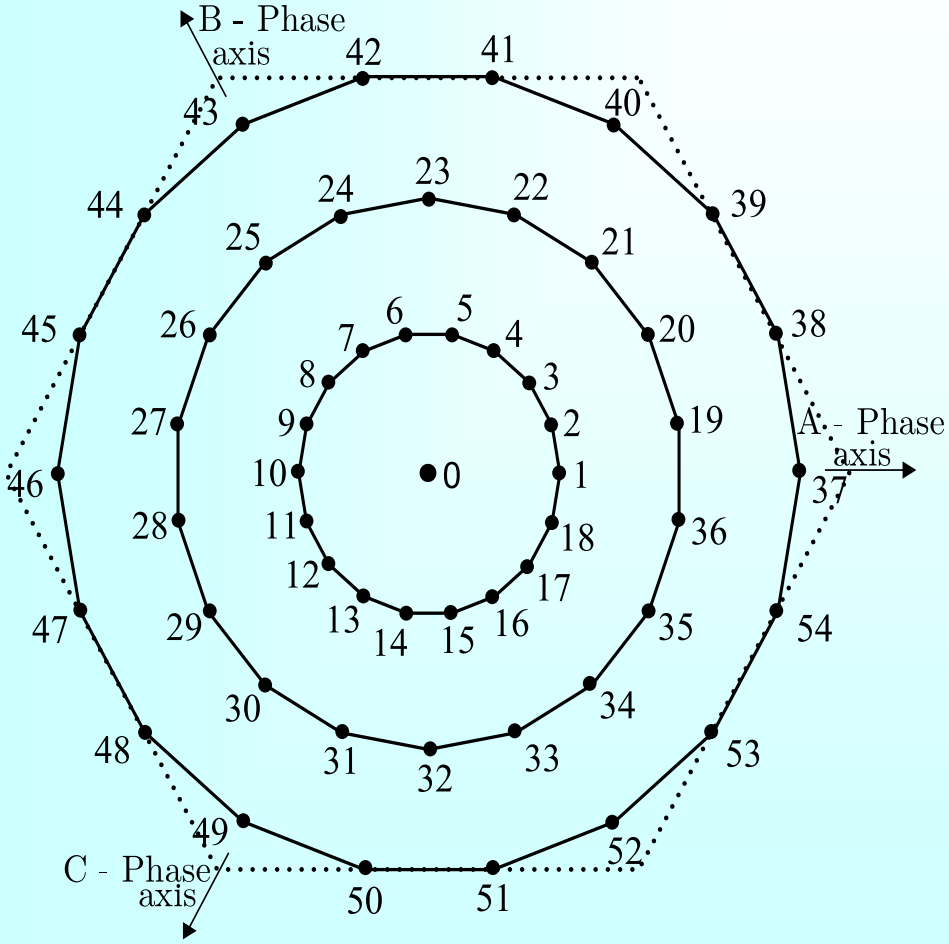
Power circuit of the proposed inverter



$$0.1207V_{dc} + 0.2266V_{dc} + 0.3473V_{dc} + 0.3054V_{dc} = 1V_{dc}$$

- Inverter 1 and Inverter 2 are three level inverters
- This topology requires an open end winding induction motor
- There are four power sources for the operation
- 12 IGBT Half Bridge modules are required for the construction

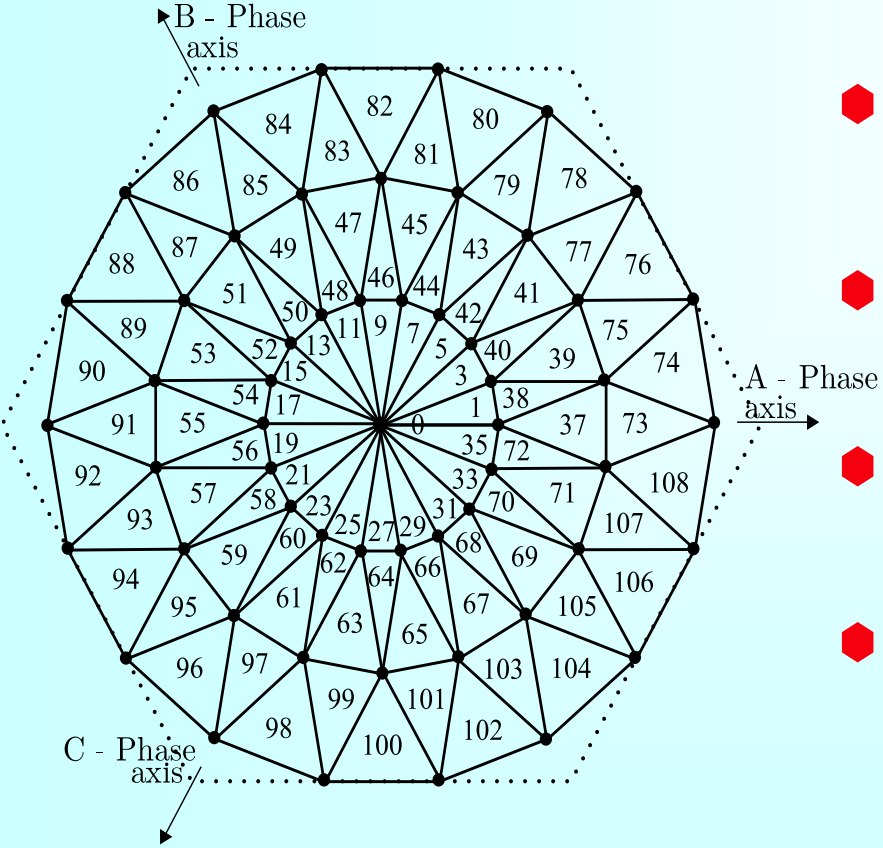
Space vector diagram



- The total number of combinations of voltage space vectors is $3^3 \times 3^3 = 729$
- Some switching points are on the vertices of 18 sided polygons
- Three 18 sided polygons are obtained with radii

  $0.305V_{dc}, 0.602V_{dc}$ and $0.879V_{dc}$
- Other than zero vector, there are 54 switching points

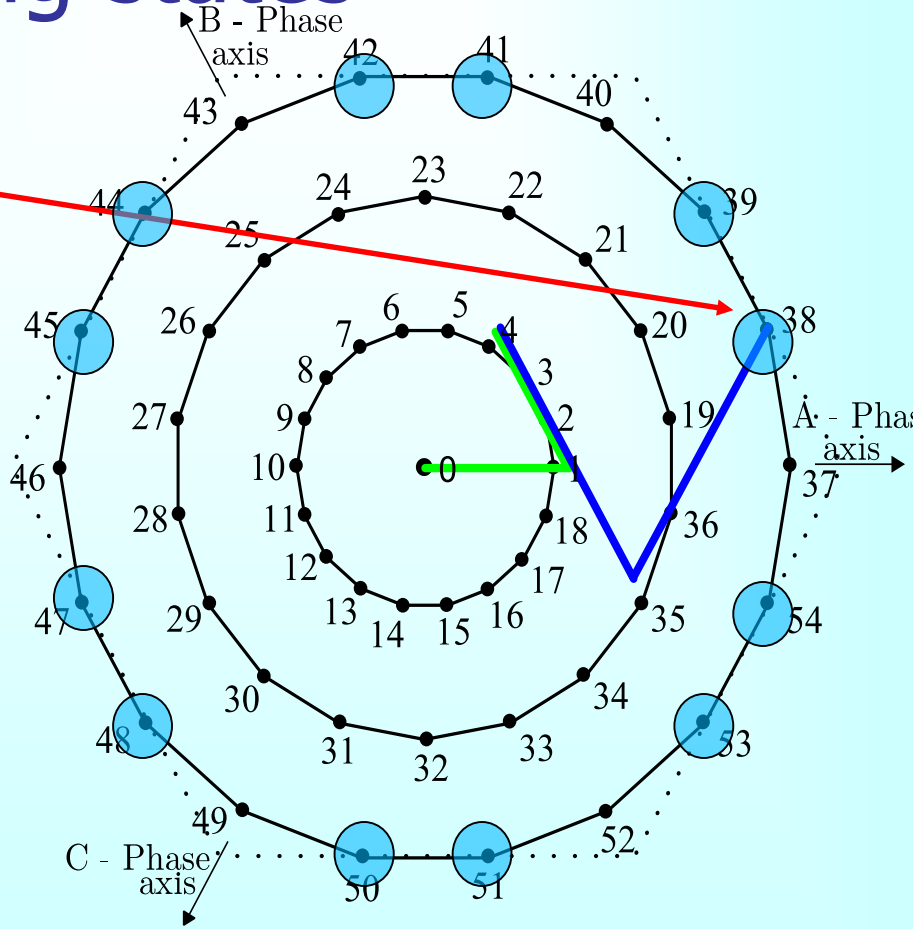
Triangular regions created by adjacent space vectors



- Adjacent 18 sided polygons can be joined to form triangles
- There are 90 isosceles triangular regions in the vector diagram
- The legs of all the triangles are same but there are 3 different base lengths
- If the tip of a reference vector is inside a triangle, the reference vector can be realized by switching between the vertices of the triangle keeping volt - second balancing

Space vector locations and the selected switching states

Points	Switching state	Points	Switching state	Points	Switching state
1	(111;122)	19	(210;122)	37	(211;022)
2	(210;111)	20	(220;011)	38	(220;022)
3	(121;011)	21	(121;012)	39	(220;012)
4	(111;112)	22	(211;102)	40	(221;002)
5	(211;101)	23	(220;101)	41	(220;102)
6	(120;111)	24	(120;212)	42	(220;202)
7	(111;212)	25	(021;212)	43	(121;202)
8	(021;111)	26	(022;101)	44	(022;202)
9	(112;101)	27	(112;201)	45	(022;201)
10	(111;211)	28	(121;210)	46	(122;200)
11	(121;110)	29	(022;110)	47	(022;210)
12	(012;111)	30	(012;221)	48	(022;220)
13	(111;221)	31	(102;221)	49	(112;220)
14	(102;111)	32	(202;110)	50	(202;220)
15	(211;110)	33	(211;120)	51	(202;120)
16	(111;121)	34	(112;021)	52	(212;020)
17	(112;011)	35	(202;011)	53	(202;021)
18	(201;111)	36	(201;122)	54	(202;022)



For these space vectors, there is no is no redundant switching states

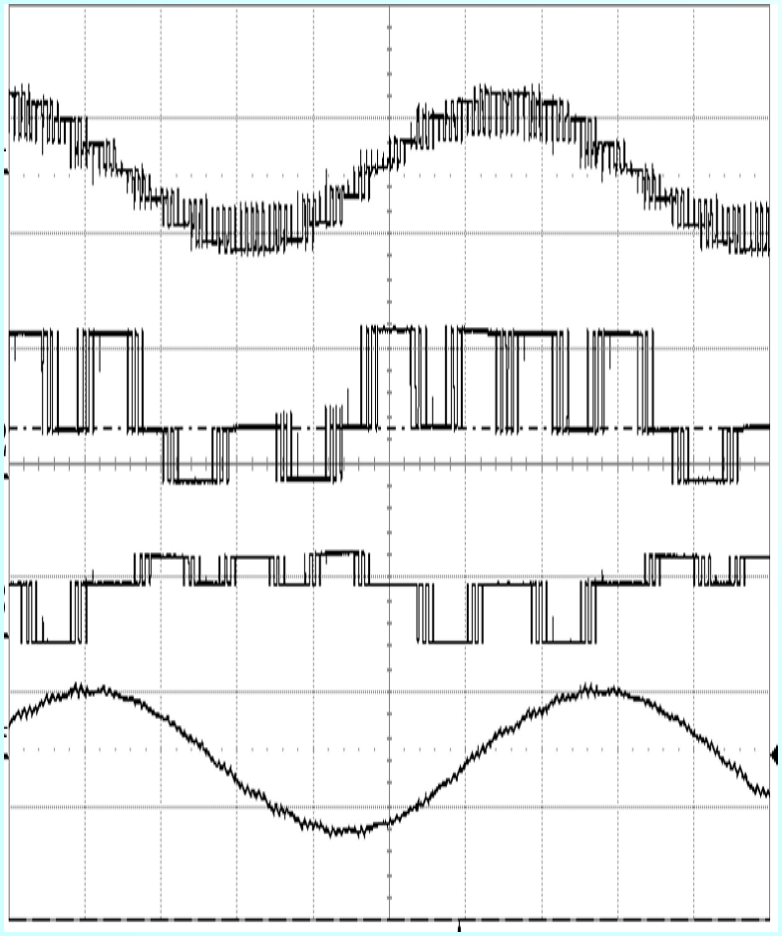
Experimental results at 30Hz operation

Phase voltage (200V/div)

Inverter1 Pole voltage (100V/div)

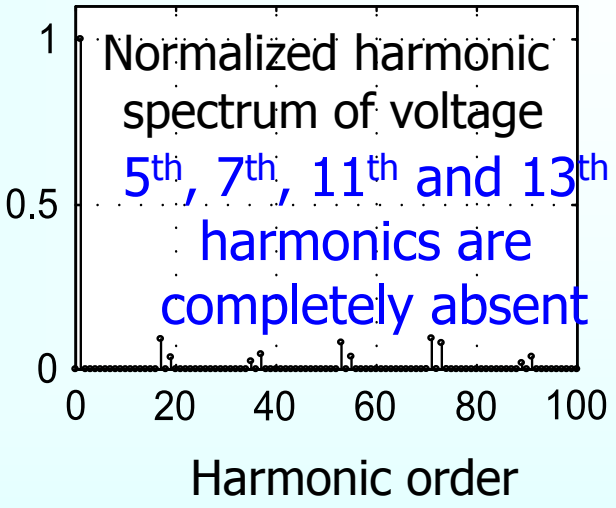
Inverter2 Pole voltage (250V/div)

Phase current (2A/div)

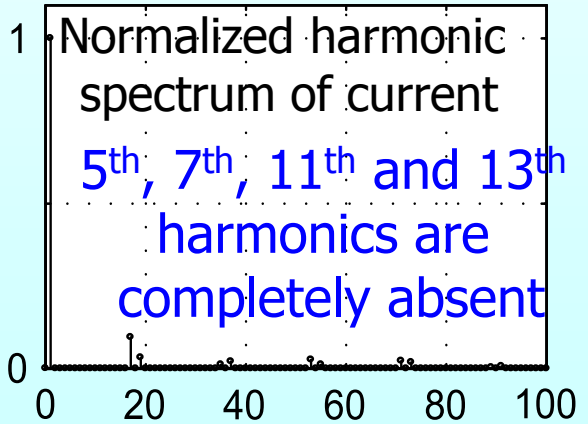


Time (5ms/div)

harmonic amplitude



harmonic amplitude



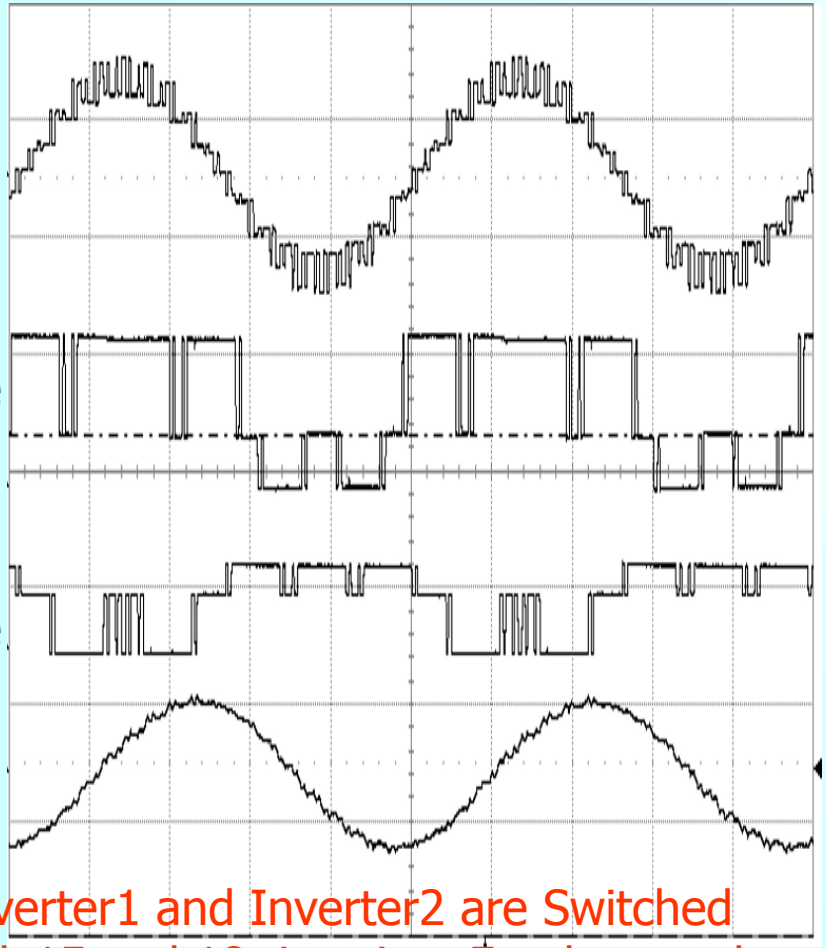
Experimental results at 40Hz operation

Phase voltage (200V/div)

Inverter1 Pole voltage (100V/div)

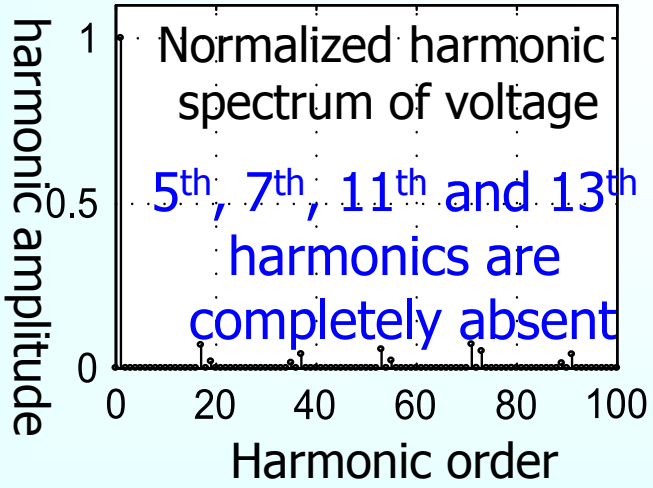
Inverter2 Pole voltage (250V/div)

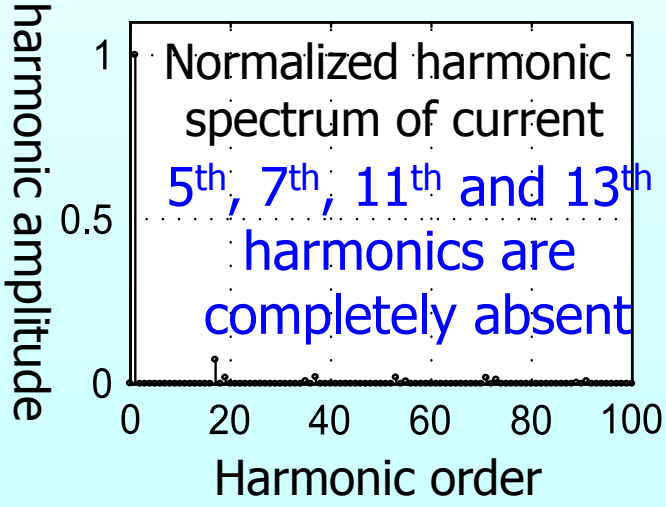
Phase current (2A/div)



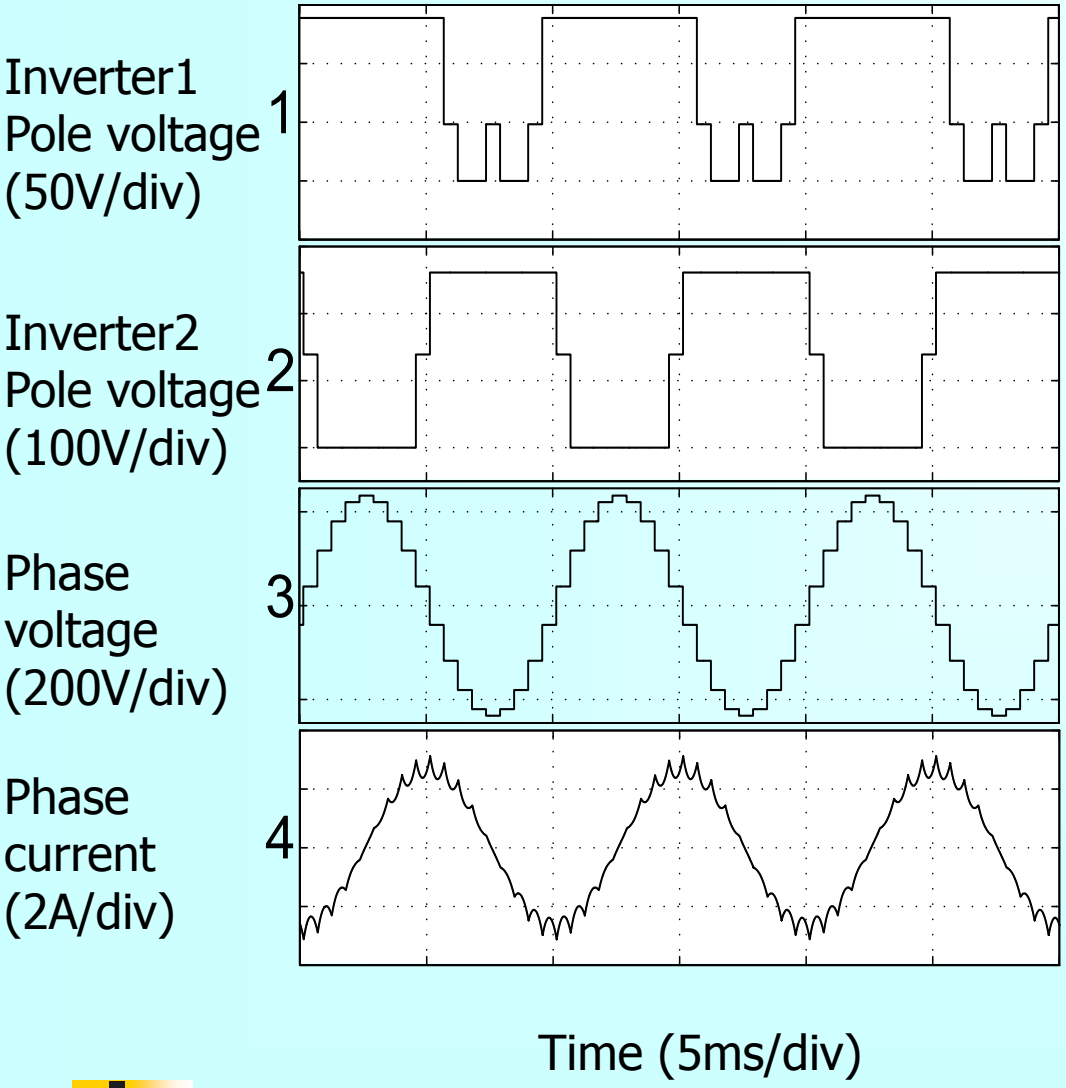
Inverter1 and Inverter2 are Switched only15 and 18 timesin a Fundamental cycle

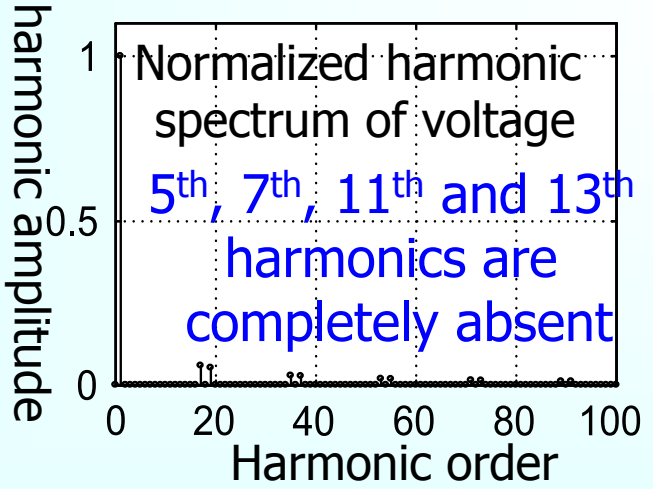
Time (5ms/div)

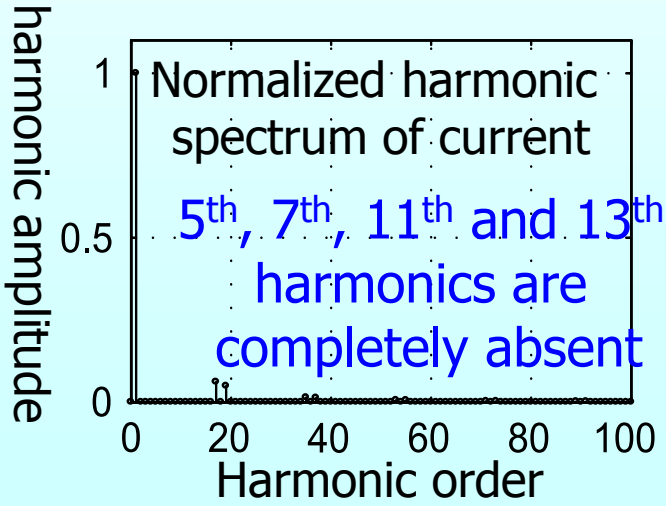




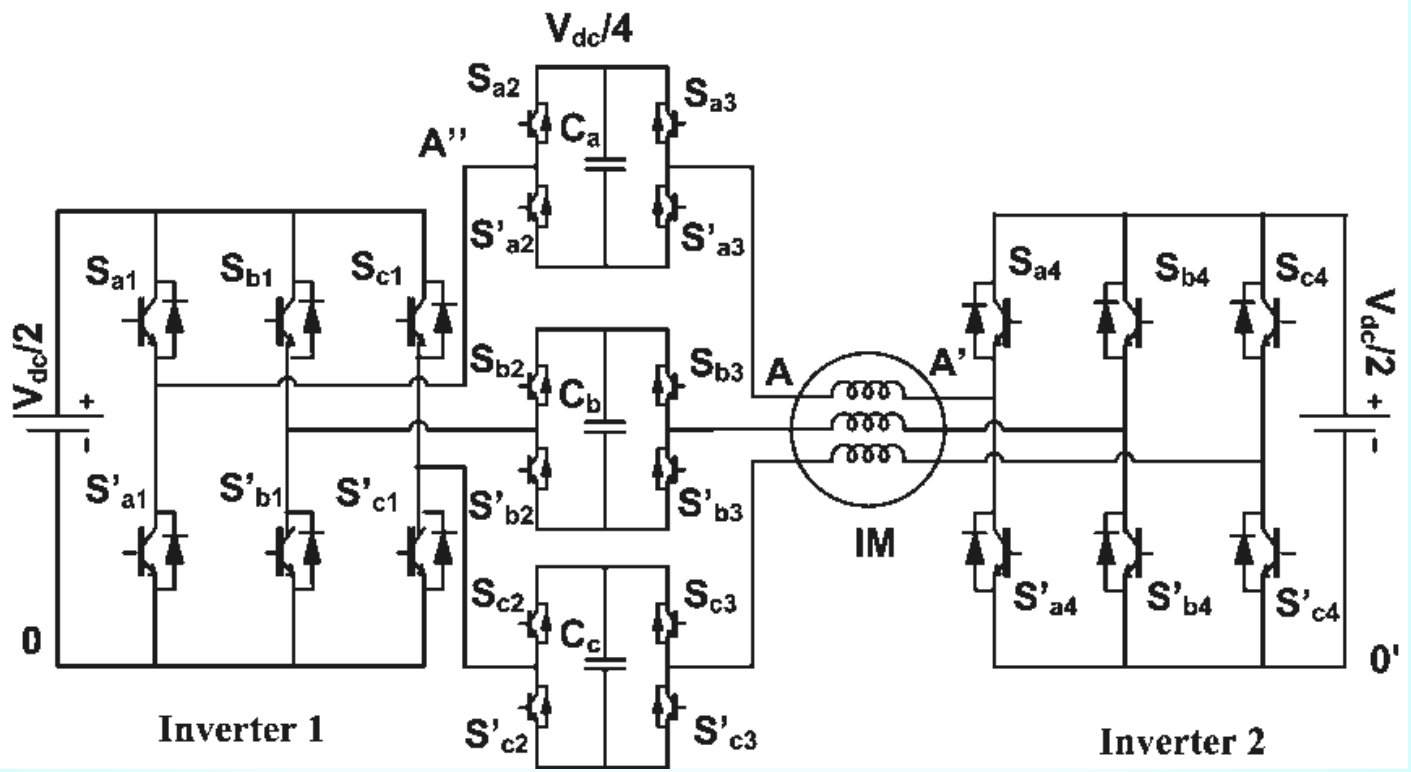
Simulation results at 50Hz operation







Hybrid multilevel inverter topology for open-ending winding induction motor



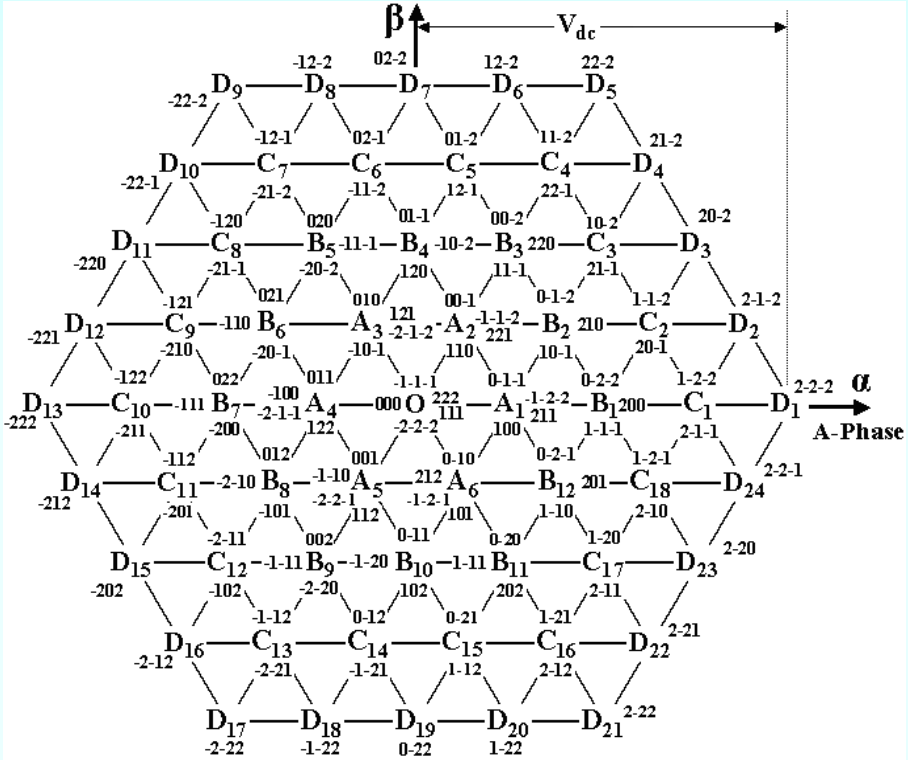
- The open-end winding concept further improved by connecting a capacitor fed H-bridge cell in series with the motor phase winding

All possible switching combinations to realize five voltage levels

Phase voltage (level)	$V_{dc}/2$ (2)		$V_{dc}/4$ (1)			0 (0)				$-V_{dc}/4$ (-1)			$-V_{dc}/2$ (-2)	
Status of S_{a1}	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
Status of S_{a2}	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF
Status of S_{a3}	ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF
Status of S_{a4}	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON
Capacitor C_a status	Ideal		$i_a>0$: charging $i_a<0$: discharging	$i_a>0$: discharging $i_a<0$: charging		Ideal				$i_a<0$: charging $i_a>0$: discharging	$i_a<0$: discharging $i_a>0$: charging		ideal	

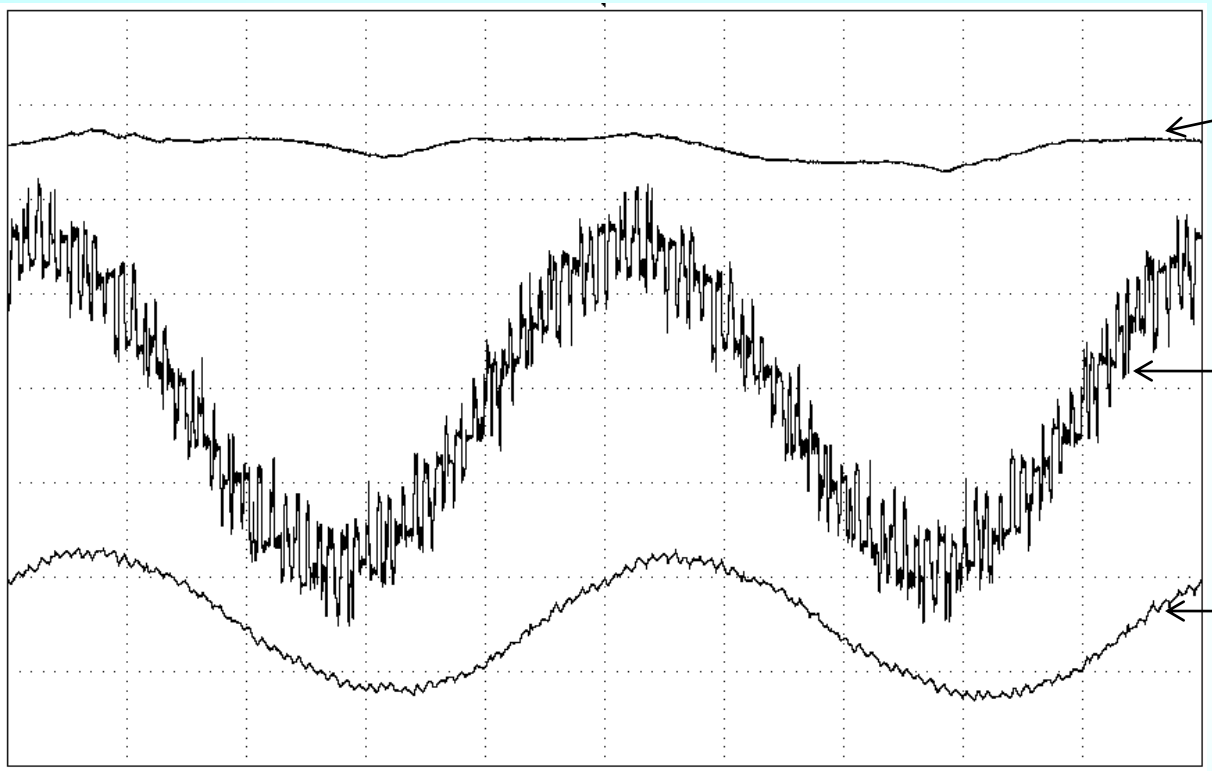
- due to the complementary nature of the two-level inverter switches, switch S_{a1} is 'ON' automatically implies that switch S'_{a1} is 'OFF'

Voltage space vector locations for a Five-level inverter



- In case of any switch failure in the capacitor fed H-bridge cell circuit, the proposed topology can still operate, for the full modulation range, as a three level inverter
- Thereby, the reliability of the system increases

Experimental results for modulation index 0.8



Flying capacitor ripple voltage [2V/div]

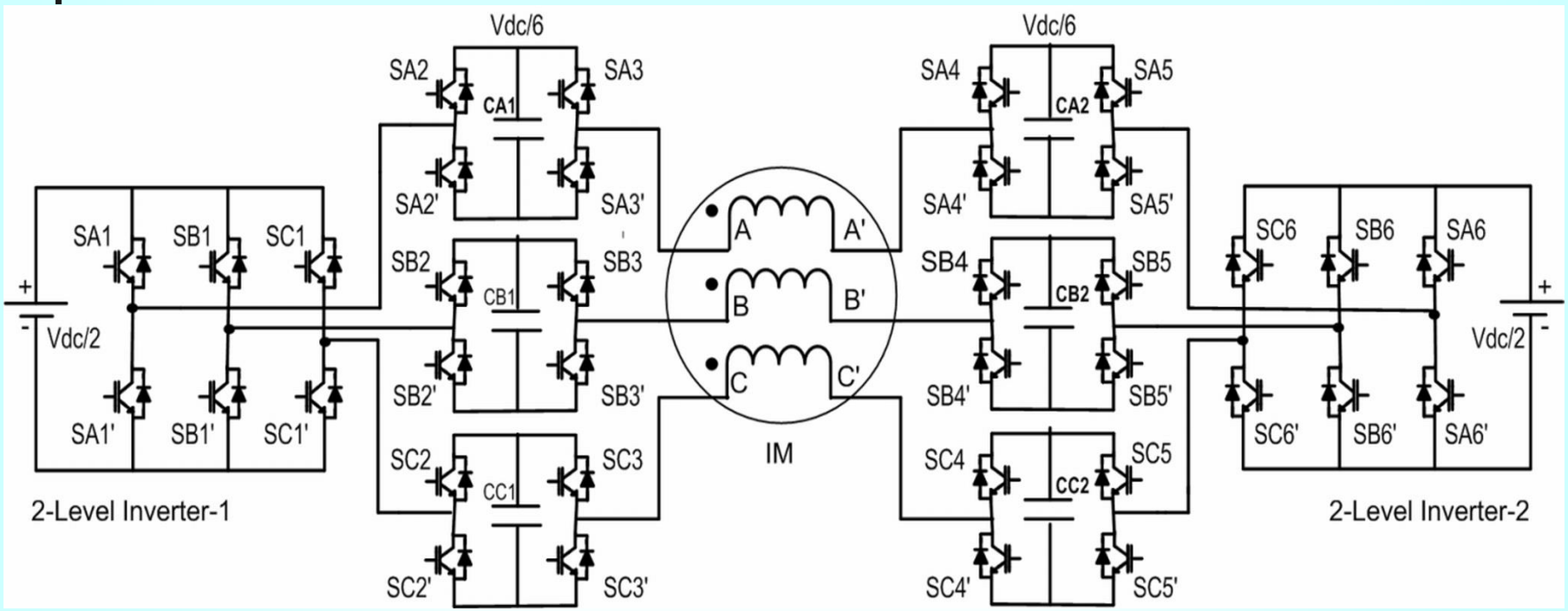
phase voltage [Y-axis: 50V/div]

phase current [Y-axis: 1A/div] [X-axis: 10ms/div]

- The flying capacitor voltage is well balanced (since, ripple voltage magnitude is less) when the inverter is operating at five-level mode

A Hybrid Seven-level Inverter with improved fault tolerance for AC Drives with open-end stator windings

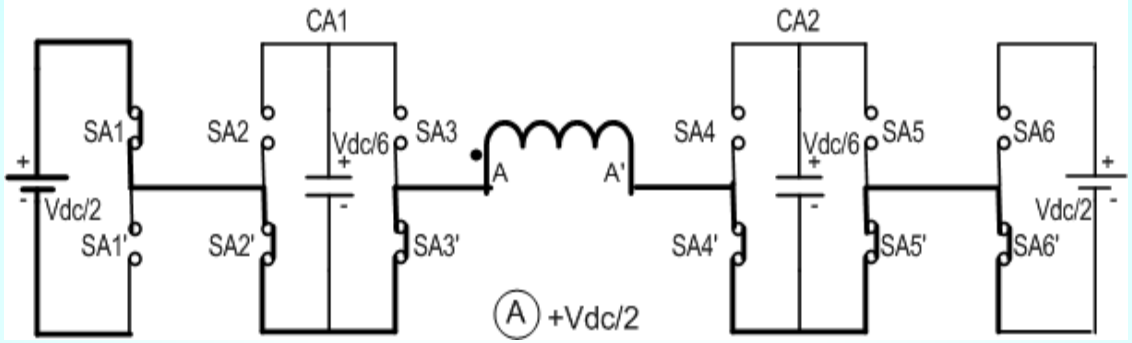
Proposed Seven-level Inverter Power circuit



- Seven voltage levels: +Vdc/2, +2Vdc/6, +Vdc/6, 0, -Vdc/6,-2Vdc/6 ,-Vdc/2

- Only two voltage sources are used with a magnitude of $V_{dc}/2$ where V_{dc} is the maximum magnitude of the voltage space vector.

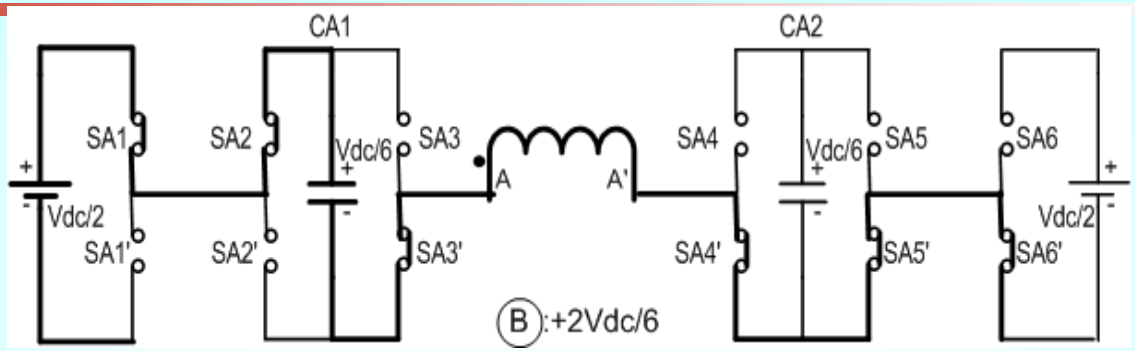
GENERATION OF +Vdc/2



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
+Vdc/2	1	1	1	0	0	0	Unaffected	Unaffected
	1	0	0	1	1	0	Unaffected	Unaffected
	1	1	1	1	1	0	Unaffected	Unaffected
	1	0	0	0	0	0	Unaffected	Unaffected

- **'1' and '0' indicate 'ON' and 'OFF' positions of the switch respectively.**
- **The switch SA1 is 'ON' automatically implies that switch S'A1 is 'OFF'**
- **Capacitor voltages are not affected by these switching states.**

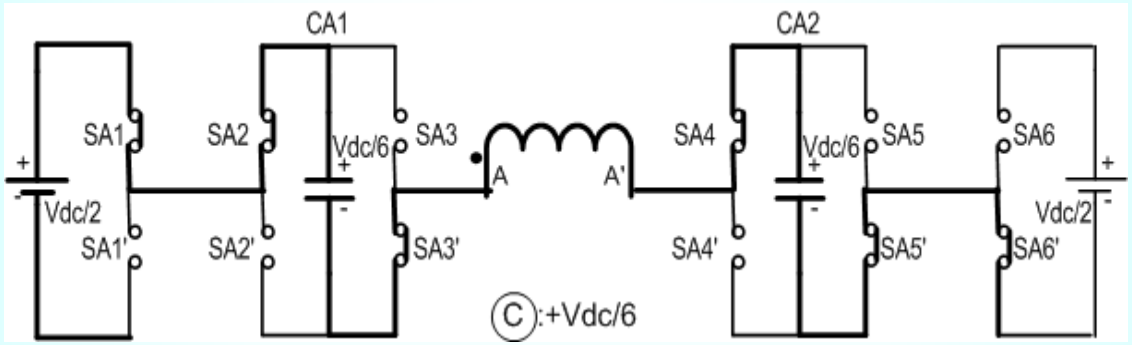
GENERATION OF +2Vdc/6



PHASE VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
+2Vdc/6	1	1	0	0	0	0	Vca1<Vdc/6 *i*a >0,charging	Vca2< or >Vdc/6 *i*a >0,status quo
	1	1	0	0	0	0	Vca1>Vdc/6 *i*a <0,discharging	Vca2< or >Vdc/6 *i*a <0,status quo
	1	0	0	1	0	0	Vca1>Vdc/6 *i*a >0, status quo	Vca2<Vdc/6 *i*a >0,charging
	1	0	0	1	0	0	Vca1<Vdc/6 *i*a <0, status quo	Vca2>Vdc/6 *i*a <0,discharging
	0	0	1	0	1	0	Vca1>Vdc/6 *i*a >0,discharging	Vca2>Vdc/6 *i*a >0,discharging
	0	0	1	0	1	0	Vca1<Vdc/6 *i*a <0,charging	Vca2<Vdc/6 *i*a <0,charging

➢**The current from A to A' is assumed to be the positive direction of current**

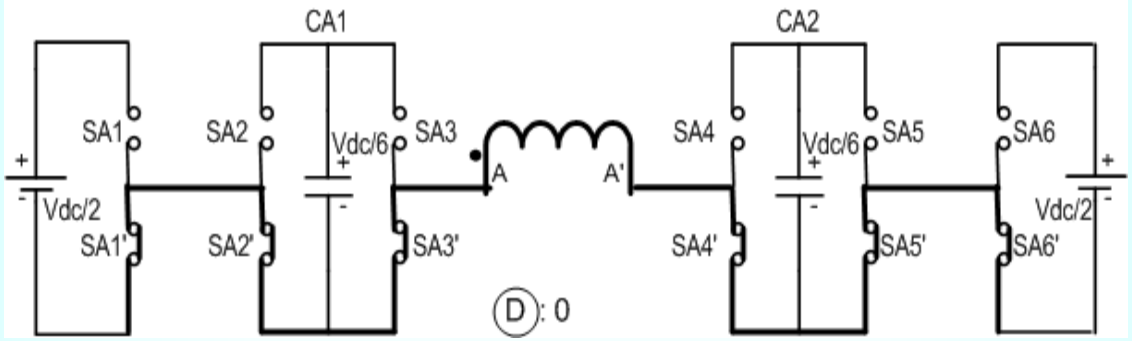
Generation of +Vdc/6



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
+Vdc/6	1	1	0	1	0	0	Vca1<Vdc/6 *i*a >0,charging	Vca2<Vdc/6 *i*a >0,charging
	1	1	0	1	0	0	Vca1>Vdc/6 *i*a <0,discharging	Vca2>Vdc/6 *i*a <0,discharging
	0	0	1	0	0	0	Vca1>Vdc/6 *i*a >0,discharging	Vca2< or >Vdc/6 *i*a >0,status quo
	0	0	1	0	0	0	Vca1<Vdc/6 *i*a <0,charging	Vca2< or >Vdc/6 *i*a <0,status quo
	0	0	0	0	1	0	Vca1<Vdc/6 *i*a >0, status quo	Vca2>Vdc/6 *i*a >0,discharging
	0	0	0	0	1	0	Vca1>Vdc/6 *i*a <0, status quo	Vca2<Vdc/6 *i*a <0,charging

The current from A to A' is assumed to be the positive direction of current

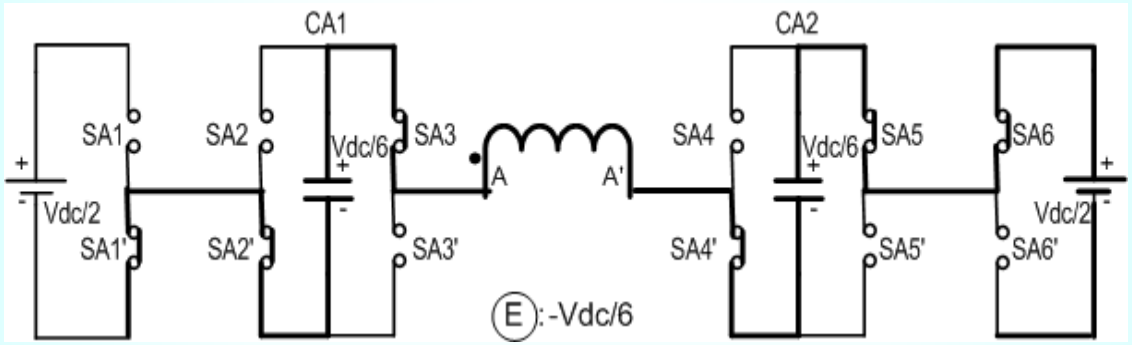
Generation of '0' Voltage level



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
0	0	0	0	0	0	0	Unaffected	Unaffected
	0	1	1	1	1	0	Unaffected	Unaffected
	0	1	1	0	0	0	Unaffected	Unaffected
	0	0	0	1	1	0	Unaffected	Unaffected
	1	0	0	0	0	1	Unaffected	Unaffected
	1	1	1	1	1	1	Unaffected	Unaffected
	1	1	1	0	0	1	Unaffected	Unaffected
	1	0	0	1	1	1	Unaffected	Unaffected

The current from A to A' is assumed to be the positive direction of current

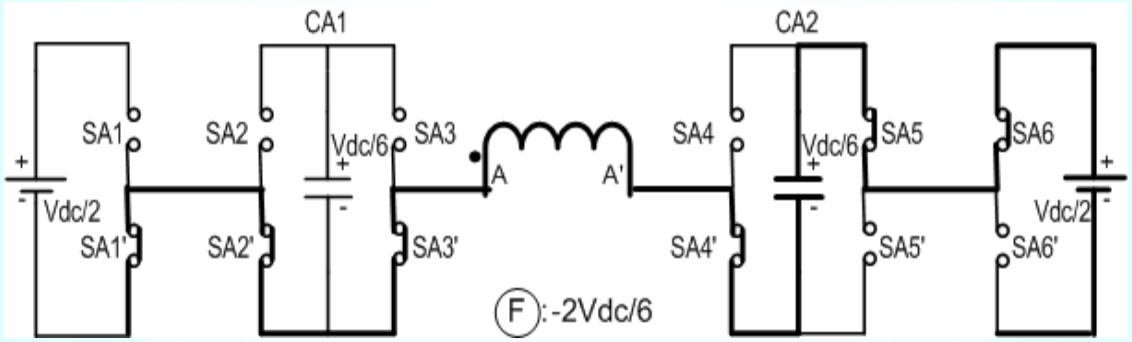
Generation of –Vdc/6



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
-Vdc/6	0	0	1	0	1	1	Vca1<Vdc/6 *i*a <0,charging	Vca2< Vdc/6 *i*a <0,charging
	0	0	1	0	1	1	Vca1>Vdc/6 *i*a >0,discharging	Vca2>Vdc/6 *i*a >0,discharging
	0	1	0	0	0	0	Vca1>Vdc/6 *i*a<0, discharging	Vca2<Vdc/6 *i*a <0, status quo
	0	1	0	0	0	0	Vca1<Vdc/6 *i*a >0, charging	Vca2>Vdc/6 *i*a >0, status quo
	0	0	0	1	0	0	Vca1< or >Vdc/6 *i*a <0, status quo	Vca2>Vdc/6 *i*a <0,discharging
	0	0	0	1	0	0	Vca1< or >Vdc/6 *i*a >0, status quo	Vca2<Vdc/6 *i*a >0,charging

The current from A to A' is assumed to be the positive direction of current

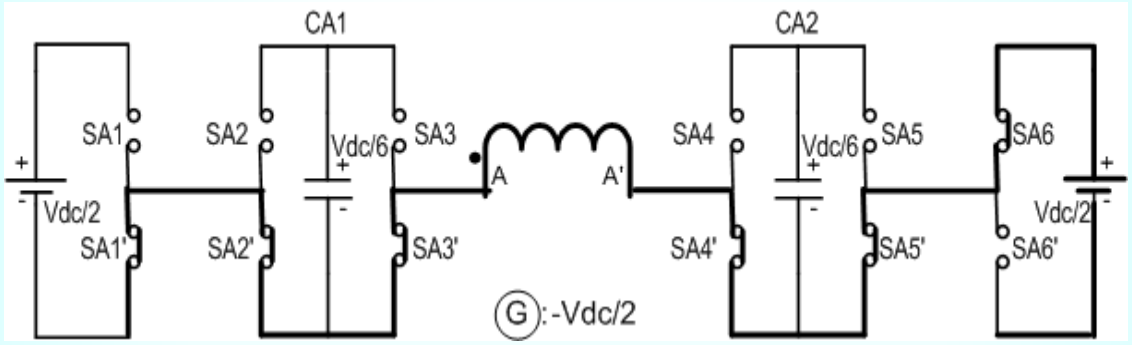
Generation of –2Vdc/6



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
-2Vdc/6	0	0	0	0	1	1	Vca1< or >Vdc/6 *i*a <0, status quo	Vca2<Vdc/6 *i*a <0,charging
	0	0	0	0	1	1	Vca1< or >Vdc/6 *i*a >0, status quo	Vca2>Vdc/6 *i*a >0,discharging
	0	0	1	0	0	1	Vca1<Vdc/6 *i*a <0,charging	Vca2>Vdc/6 *i*a <0,status quo
	0	0	1	0	0	1	Vca1>Vdc/6 *i*a >0,discharging	Vca2<Vdc/6 *i*a >0,status quo
	0	1	0	1	0	0	Vca1>Vdc/6 *i*a<0, discharging	Vca2>Vdc/6 *i*a <0,discharging
	0	1	0	1	0	0	Vca1<Vdc/6 *i*a >0, charging	Vca2<Vdc/6 *i*a >0,charging

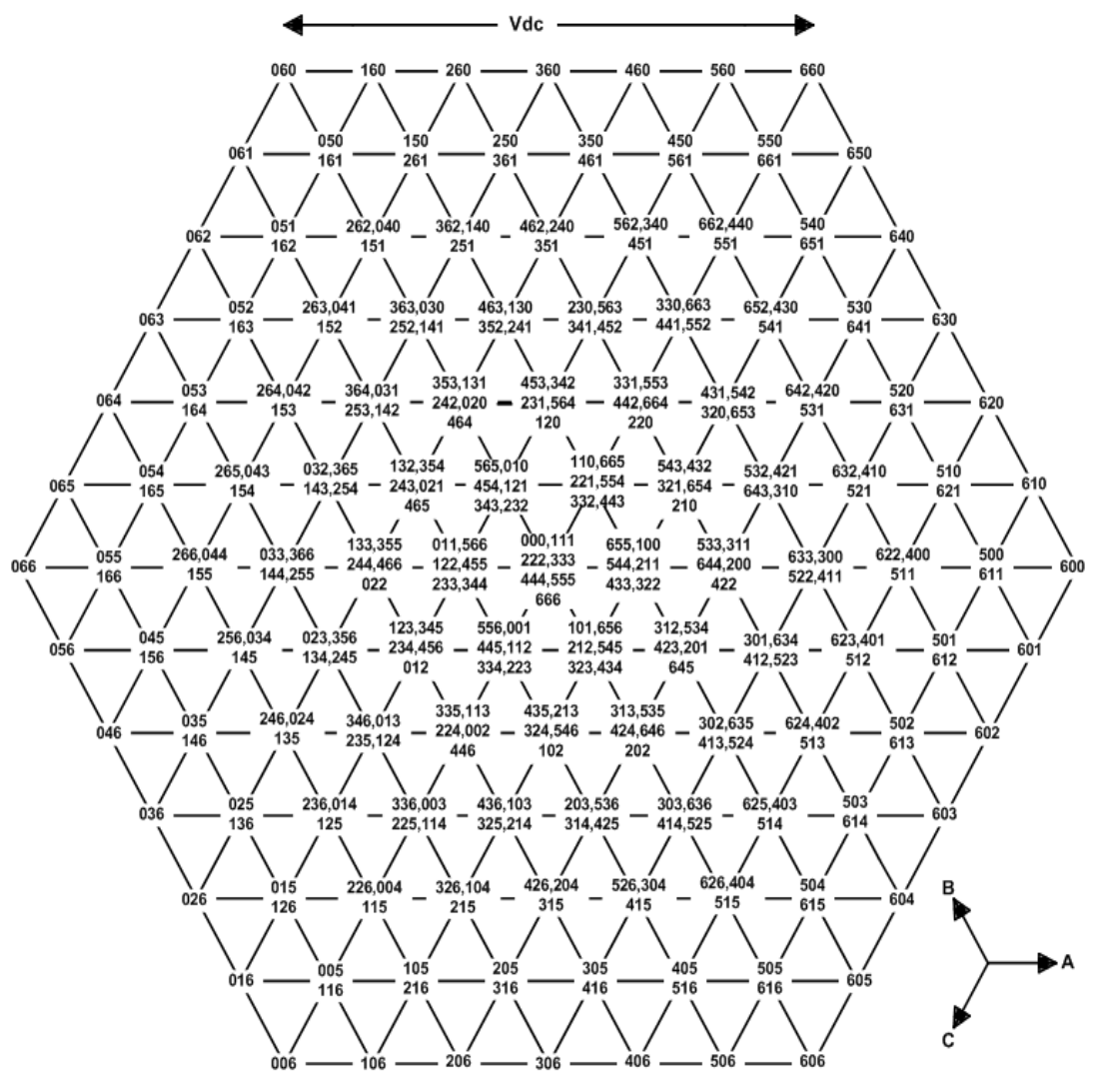
The current from A to A' is assumed to be the positive direction of current

Generation of –Vdc/2



PHASE VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
-Vdc/2	0	0	0	0	0	1	Unaffected	Unaffected
	0	1	1	1	1	1	Unaffected	Unaffected
	0	1	1	0	0	1	Unaffected	Unaffected
	0	0	0	1	1	1	Unaffected	Unaffected

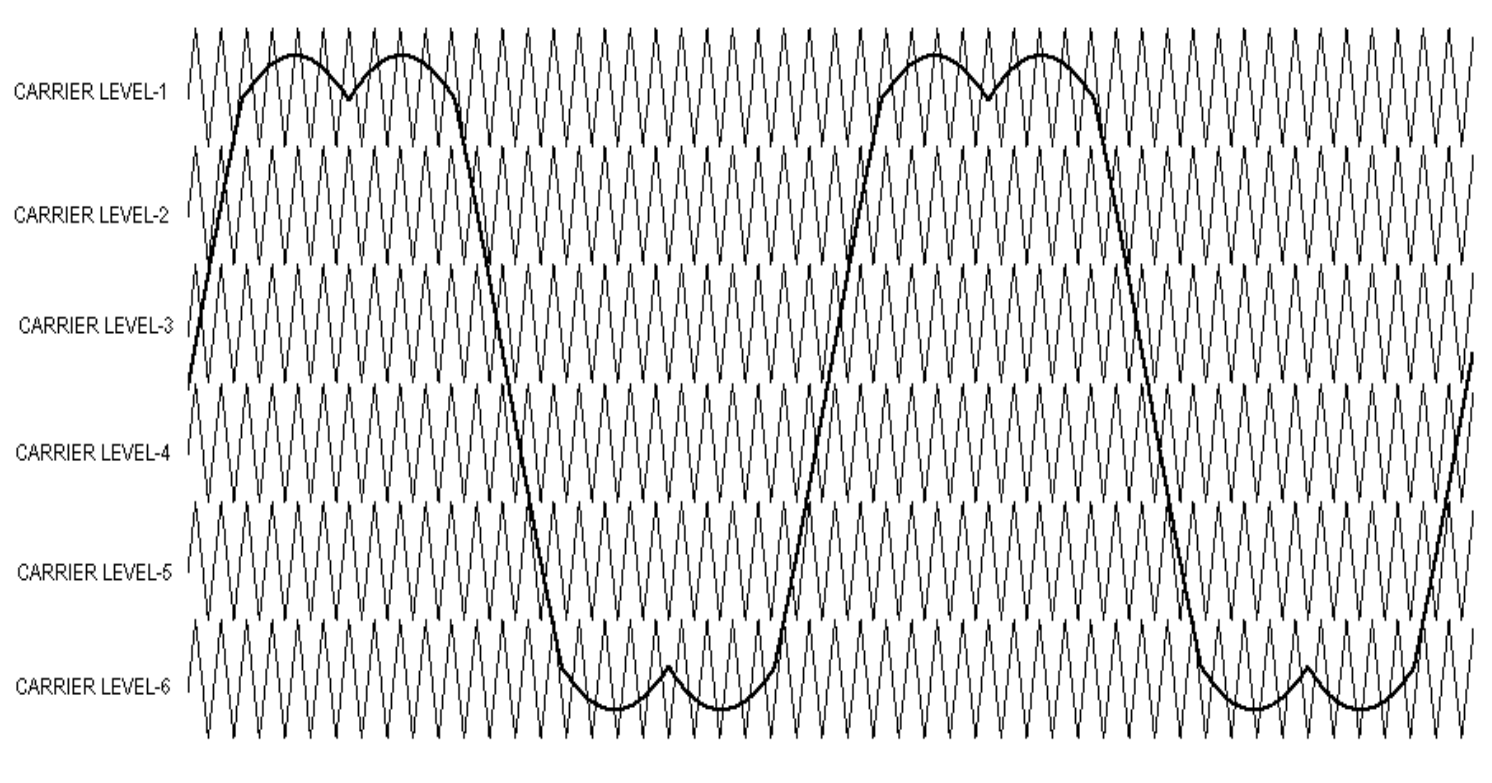
Space Vector diagram of the seven-level Inverter



Multiplicity of switching states to realize a space vector position reduces from innermost hexagon to outermost hexagon.

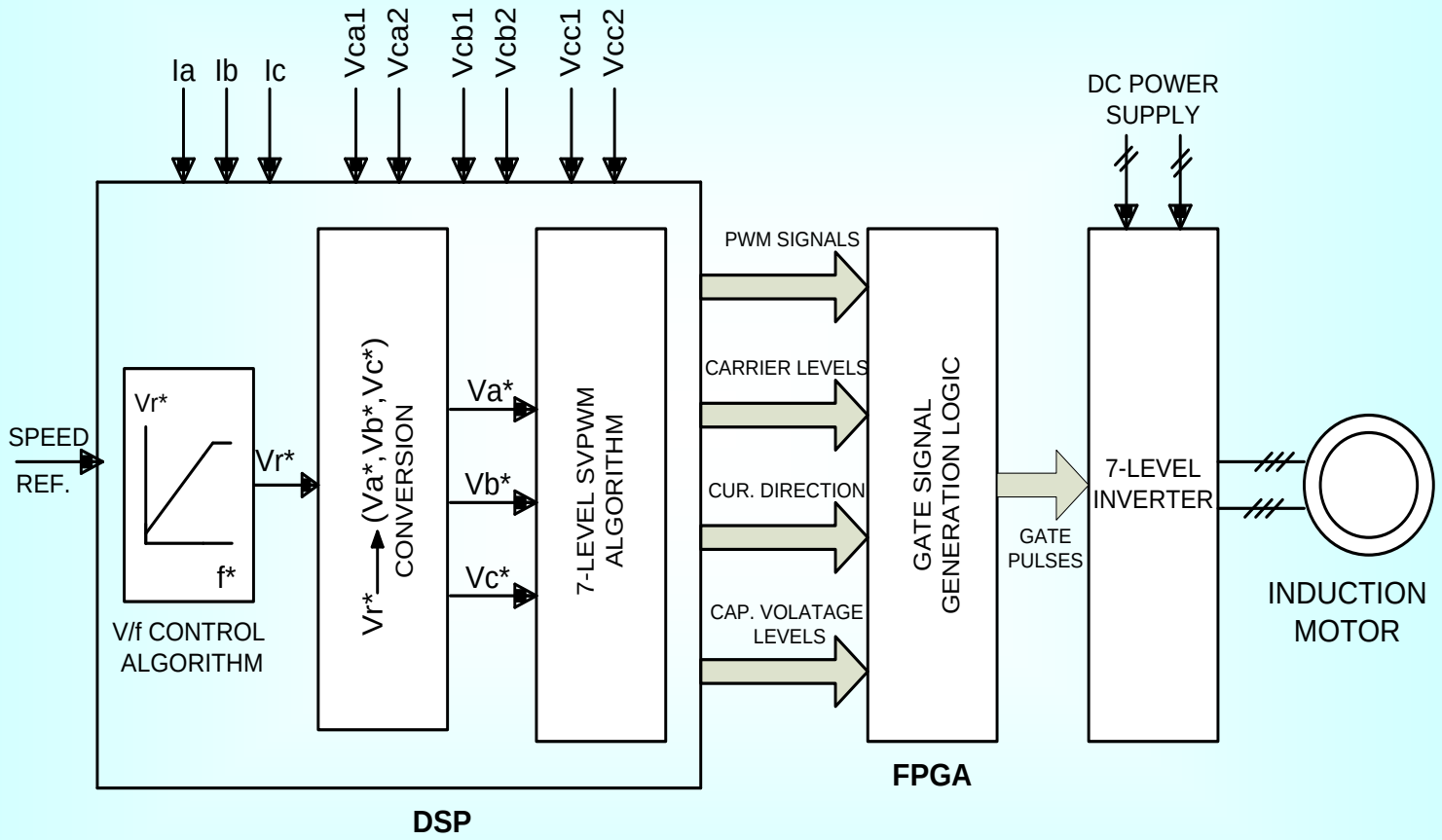
3, 2, 1, 0, -1, -2, -3 represents Vdc/2, 2Vdc/6, Vdc/6, 0, -Vdc/6, -Vdc/6 & -Vdc/2 respectively

Reference voltage waveform (after addition of V offset) and six level shifted triangular carriers

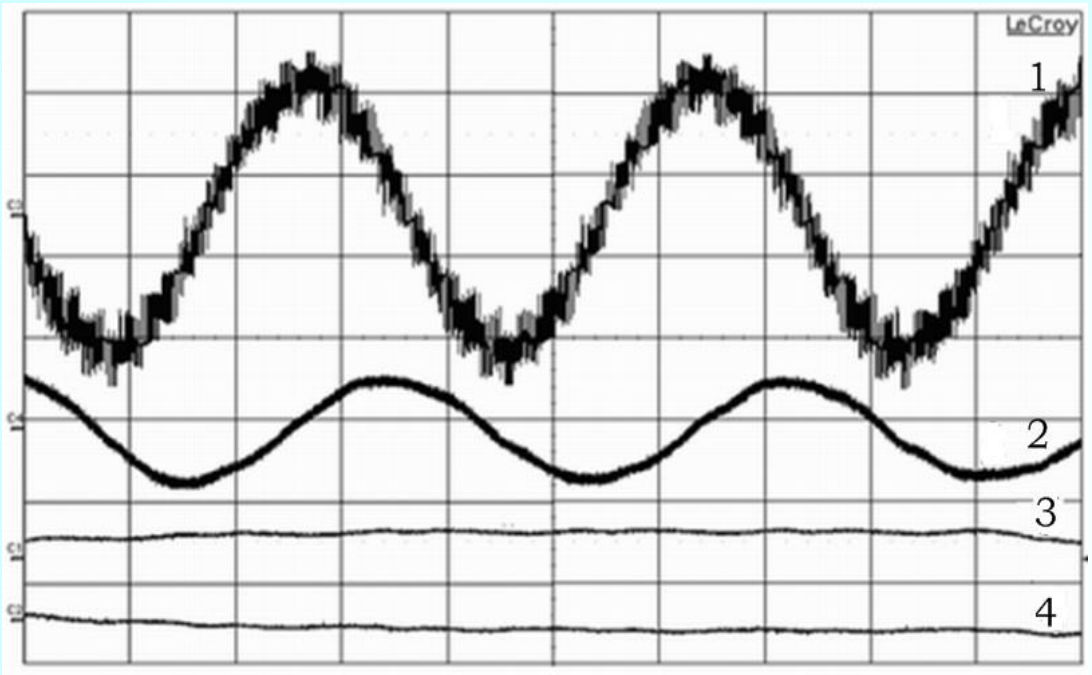


The reference voltage for M=0.8 spans all the six level shifted triangular carriers. This reference voltage waveform is compared with the triangular carrier waveforms to generate the PWM signals.

Schematic diagram of the experimental set-up.



Experimental results for modulation index 0.53



[X-axis: 10ms/div]

1.Phase voltage
[Y- axis: 100V/div]

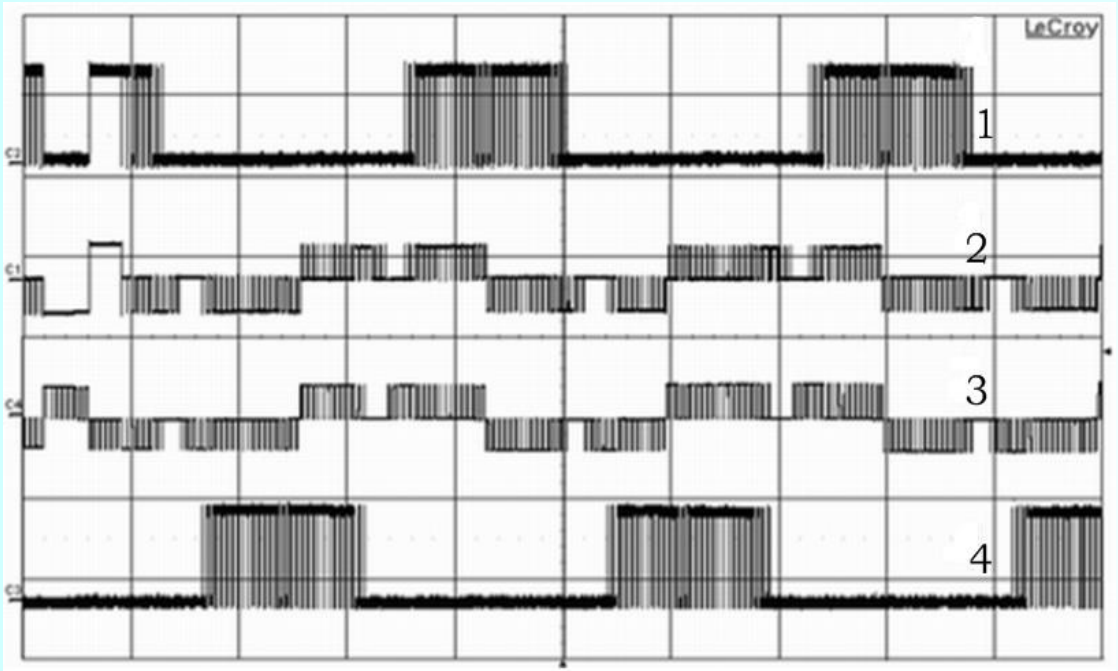
2. Phase current
[Y-axis: 2A/div]

3. H-bridge capacitor ripple voltage-V_{CA1}
[Y-axis: 10V/div]

4. H-bridge capacitor ripple voltage-V_{CA2}
[Y-axis: 10V/div]

- Five-level operation of the Inverter
- 26 Hz operation of the motor.
- The flying capacitor peak to peak voltage ripple is less than 2V

Pole voltage waveforms for modulation index 0.53

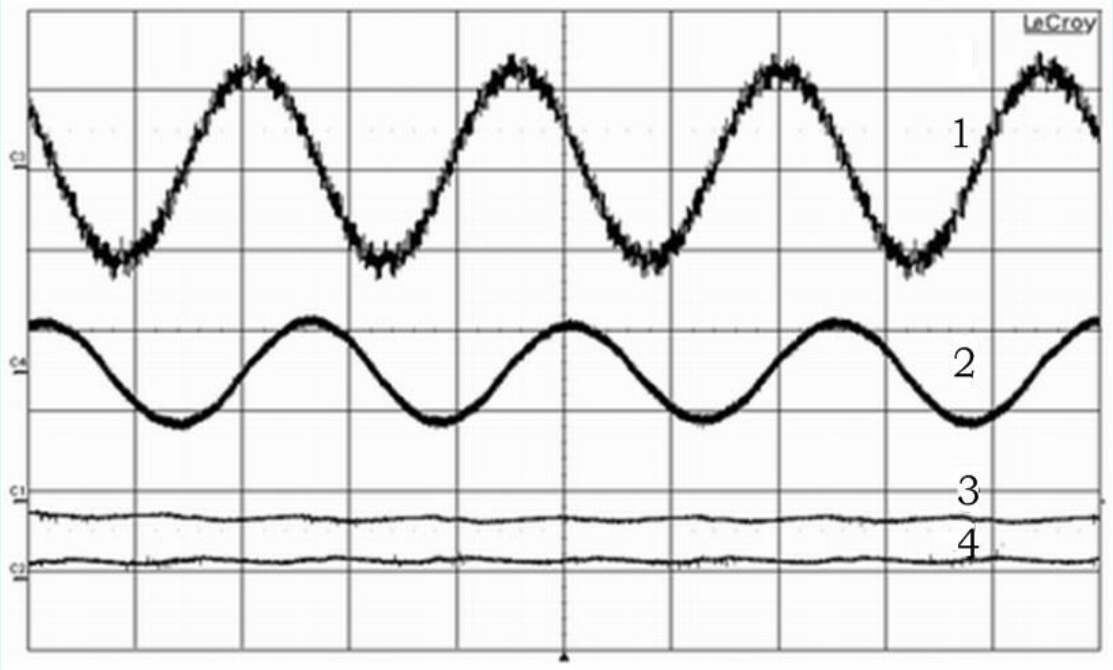


1. 2-level Inverter-1
2. H-bridge cell CA1
3. H-bridge cell CA1
4. 2-level Inverter-2

X-axis: 10ms/div
Y-axis: 200V/div

- High voltage fed inverters (i.e. inverter-1 and inverter-2) are switching half of the period in fundamental cycle
- So this will reduce the switching losses of the drive

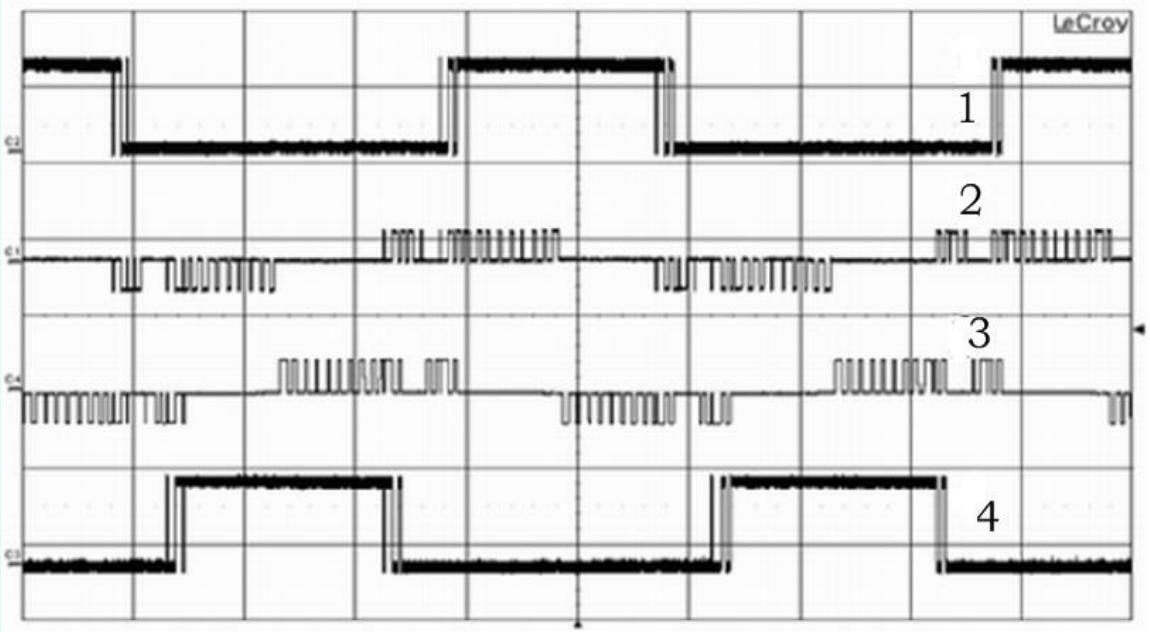
Experimental results for modulation index 0.8



1. **A-phase voltage (Y axis:200V/div).**
2. **A-phase current (Y axis :2A/div).**
3. **Ripple in H-bridge capacitor voltage Vca1 (Y axis :5V/div).**
4. **Ripple of H-bridge capacitor voltage Vca2 (Y axis :5V/div).**
   X-axis : 10ms/div

- Seven-level operation of the Inverter
- 40Hz operation of the motor.
- The flying capacitor peak to peak voltage ripple is less than 2V

Pole Voltage waveforms for modulation index 0.8



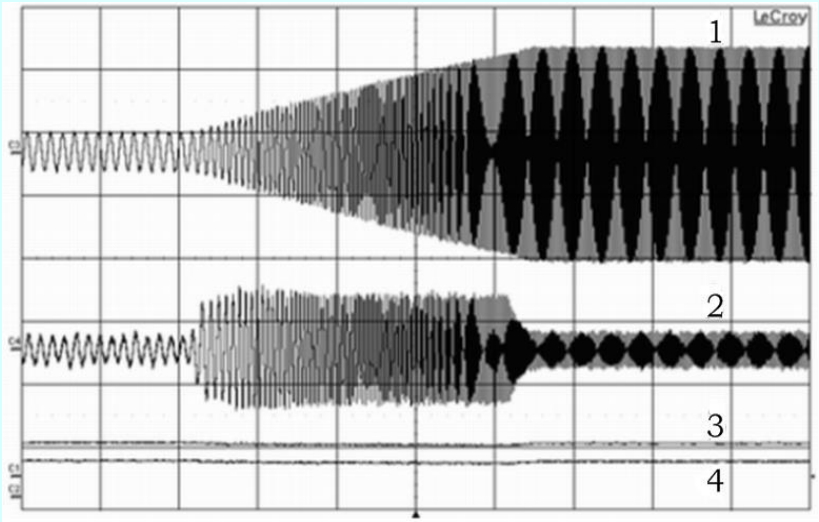
1. 2-level Inverter-1
2. H-bridge cell CA1
3. H-bridge cell CA1
4. 2-level Inverter-2

X-axis: 5ms/div

Y-axis: 200V/div

- High voltage fed inverters (i.e. inverter-1 and inverter-2) are switching half of the period in fundamental cycle
- Results in reduction in switching loss and improvement in effeiciency of the drive.

Transient performance

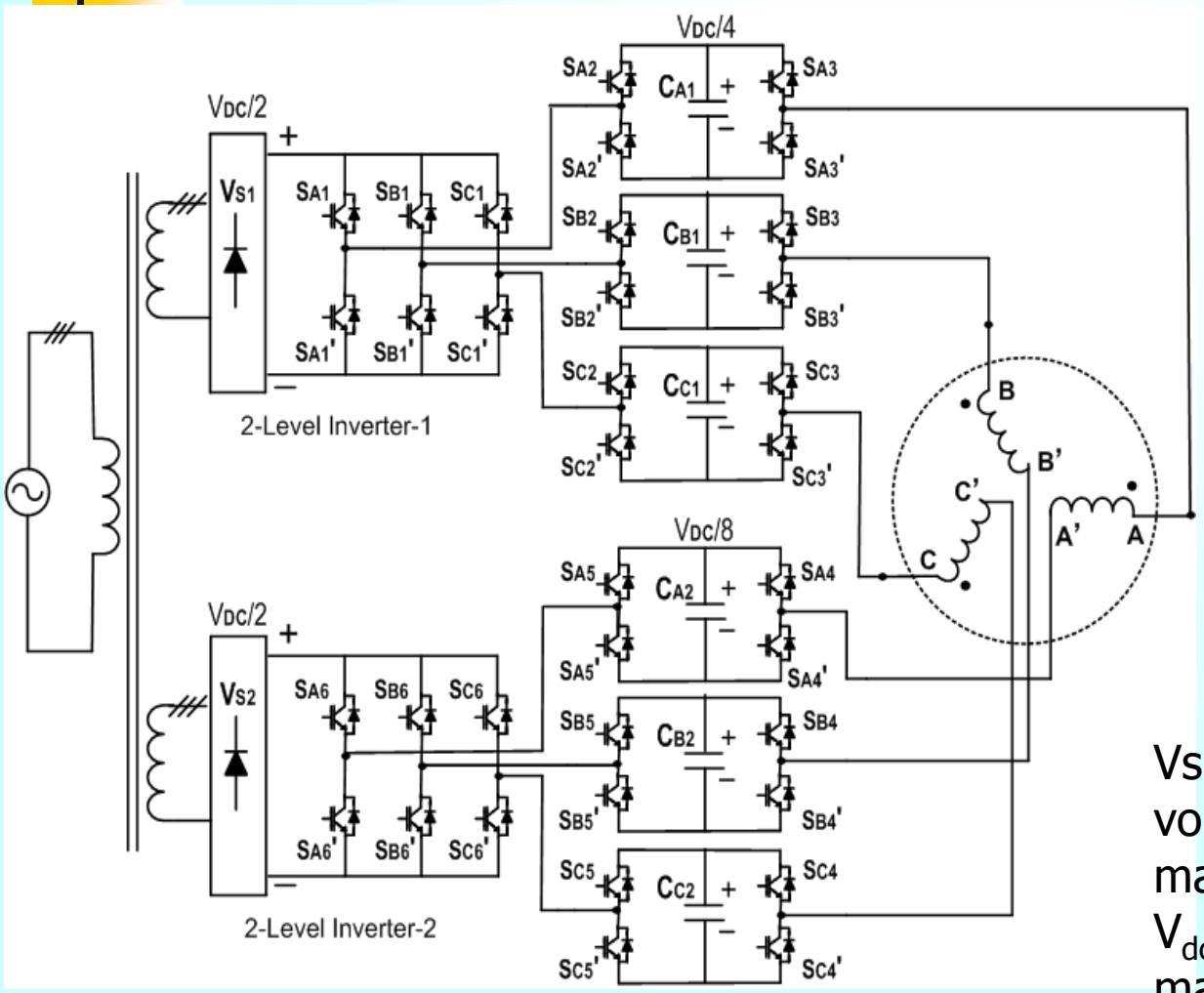


1. **A-phase voltage (Y axis:100V/div).**
2. **A-phase current (Y axis :2A/div).**
3. **Ripple in H-bridge capacitor voltage Vca1 (Y axis:100V/div).**
4. **Ripple of H-bridge capacitor voltage Vca2 (Y axis:100V/div).**

- Transient performance during acceleration of the drive
- Even though the accelerating the motor draws current much more than the steady state operation, the capacitor voltage is balanced for the full modulation range.
- Smooth transition from 6.5 Hz to 40 Hz operation corresponding to transition from two-level to seven-level operation.

A Reduced Device-count Nine-level voltage space vector generation scheme for AC drives with open-end stator windings.

Proposed Nine-level Inverter fed IM Drive



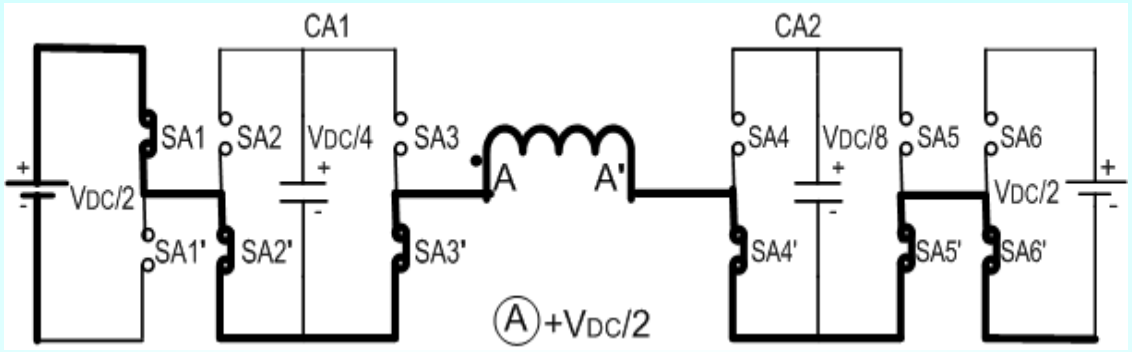
Power Circuit diagram

Nine voltage levels:

+Vdc/2
+3Vdc/8
+2Vdc/8
+Vdc/8
0
-Vdc/8
-2Vdc/8
-3Vdc/8
-Vdc/2

Vs1 and Vs2 are isolated voltage sources of magnitude of $V_{dc}/2$, where V_{dc} is the maximum magnitude of the voltage space vector.

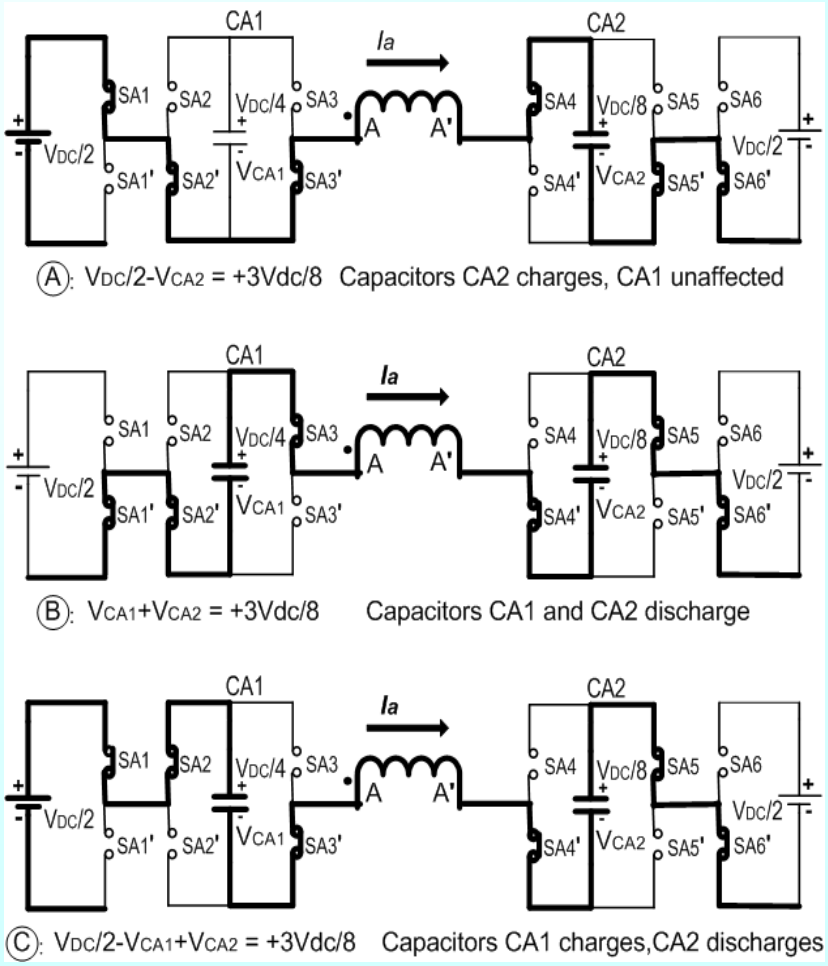
Generation of +Vdc/2 in phase-A



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
+Vdc/2	1	1	1	0	0	0	Unaffected	Unaffected
	1	0	0	1	1	0	Unaffected	Unaffected
	1	1	1	1	1	0	Unaffected	Unaffected
	1	0	0	0	0	0	Unaffected	Unaffected

- **'1' and '0' indicate 'ON' and 'OFF' positions of the switch respectively.**
- **The switch SA1 is 'ON' automatically implies that switch SA1′ is 'OFF'**
- **Capacitor voltages are not affected by these switching states.**

Generation of +3Vdc/8 and the effects on capacitors in phase-A



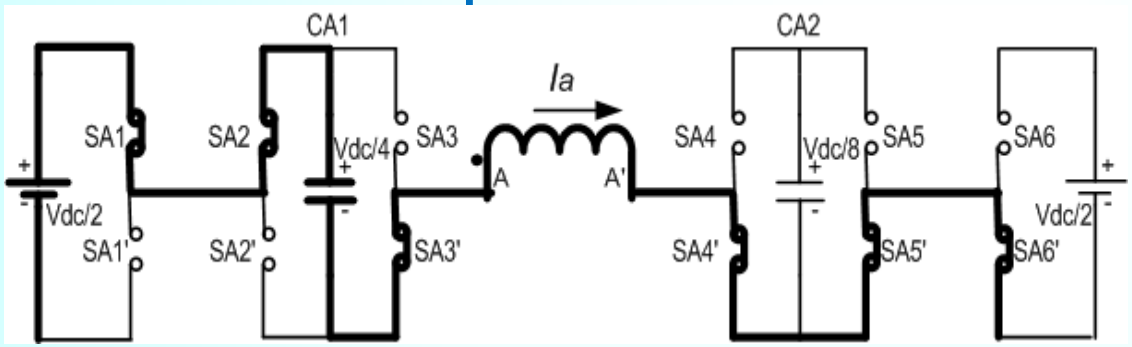
→ **Capacitors CA2 charges, CA1 unaffected**

→ **Capacitors CA1 discharges, CA2 discharges**

→ **Capacitors CA1 charges, CA2 discharges**

Charging and the discharging of the capacitors are possible in any direction of the current by proper selection of the method of generation.

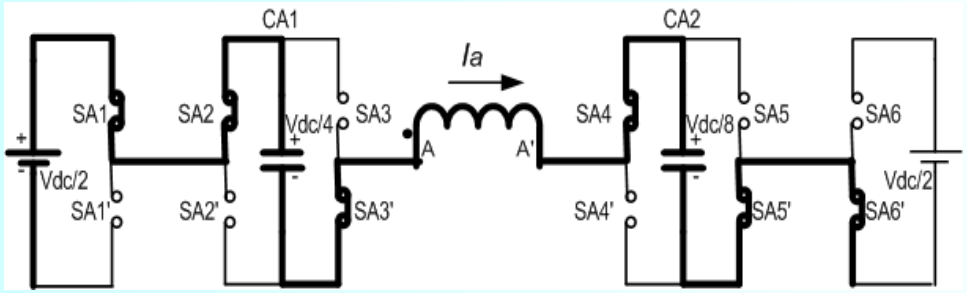
Switch-states for generation of +2Vdc/8 in phase-A



VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
+2Vdc/8	1	1	0	0	0	0	V_{CA1}<Vdc/4,*ia*>0, charging	V_{CA2}<or>Vdc/8, *ia*>0,status quo
	1	1	0	0	0	0	V_{CA1}>Vdc/4,*ia*<0, discharging	V_{CA2}<or>Vdc/8, *ia*<0,status quo
	0	0	1	0	0	0	V_{CA1}>Vdc/4,*ia*>0, discharging	V_{CA2}<or>Vdc/8, *ia*>0,status quo
	0	0	1	0	0	0	V_{CA1}<Vdc/4, *ia* <0, charging	V_{CA2}<or>Vdc/8, *ia*<0,status quo

- **The current from A to A' is assumed to be the positive direction of current. Similar methods are used for generation of +2Vdc/8 in other two phases. '1' and '0' indicate 'ON' and 'OFF' positions of the switch respectively.**

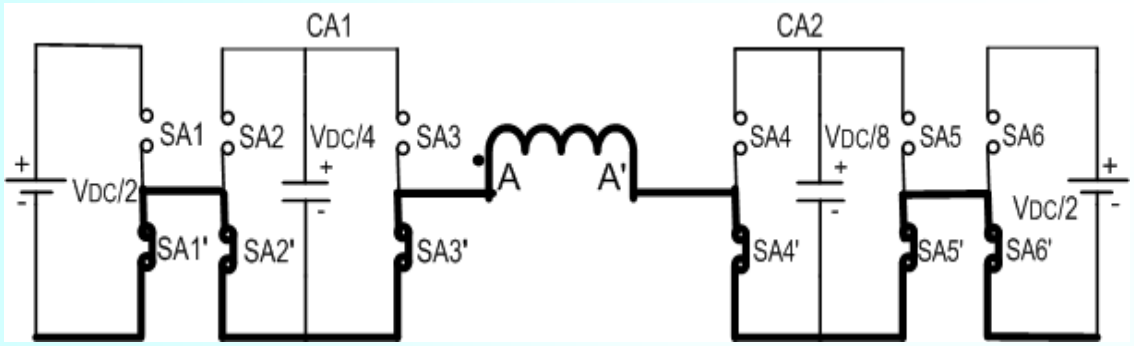
Switch-states for generation of +Vdc/8 in phase-A



VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
+Vdc/8	1	1	0	1	0	0	V_{CA1}<Vdc/4, *i*a>0, charging	V_{CA2}<Vdc/8, *i*a>0, charging
	1	1	0	1	0	0	V_{CA1}>Vdc/4, *i*a<0, discharging	V_{CA2}>Vdc/8, *i*a<0, discharging
	0	0	1	1	0	0	V_{CA1}>Vdc/4, *i*a >0, discharging	V_{CA2}<Vdc/8, *i*a>0, charging
	0	0	1	1	0	0	V_{CA1}<Vdc/4, *i*a <0, charging	V_{CA2}>Vdc/8, *i*a<0, discharging
	0	0	0	0	1	0	V_{CA1}<or>Vdc/4, *i*a>0,status quo	V_{CA2}>Vdc/8, *i*a >0, discharging
	0	0	0	0	1	0	V_{CA1}<or>Vdc/4, *i*a<0, status quo	V_{CA2}<Vdc/8, *i*a <0, charging

- **The current from A to A′ is assumed to be the positive direction of current. Similar methods are used for generation of +Vdc/8 in other two phases. '1' and '0' indicate 'ON' and 'OFF' positions of the switch respectively.**

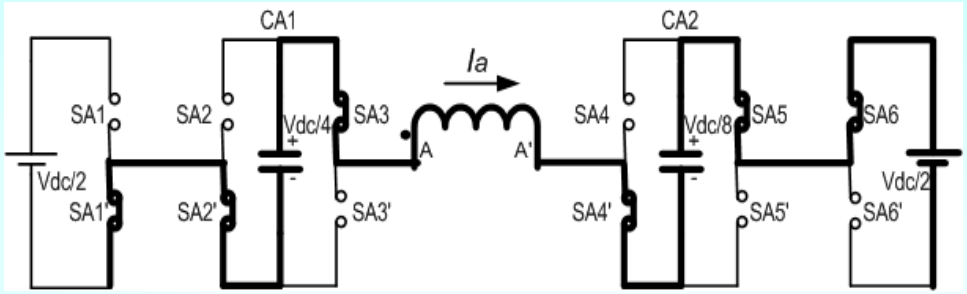
Generation of '0' Voltage level



PHASE VOLTAGE LEVELS	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
0	0	0	0	0	0	0	Unaffected	Unaffected
	0	1	1	1	1	0	Unaffected	Unaffected
	0	1	1	0	0	0	Unaffected	Unaffected
	0	0	0	1	1	0	Unaffected	Unaffected
	1	0	0	0	0	1	Unaffected	Unaffected
	1	1	1	1	1	1	Unaffected	Unaffected
	1	1	1	0	0	1	Unaffected	Unaffected
	1	0	0	1	1	1	Unaffected	Unaffected

The capacitor voltages are not affected.

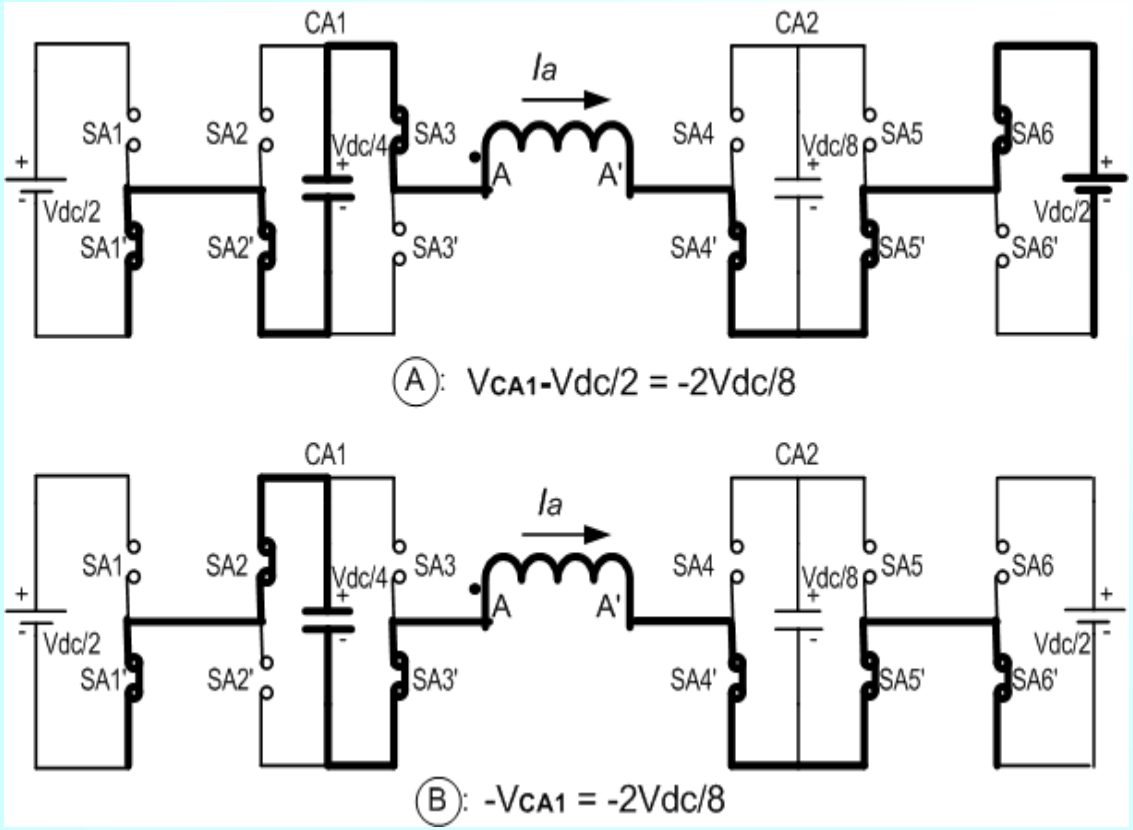
Switch-states for generation of –Vdc/8



VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
-Vdc/8	0	0	1	0	1	1	V_{CA1}>Vdc/4,*i*a>0, discharging	V_{CA2}>Vdc/8, *i*a>0, discharging
	0	0	1	0	1	1	V_{CA1}<Vdc/4,*i*a<0, charging	V_{CA2}<Vdc/8, *i*a<0, charging
	0	1	0	0	1	0	V_{CA1}<Vdc/4, *i*a >0, charging	V_{CA2}>Vdc/8, *i*a>0, discharging
	0	1	0	0	1	0	V_{CA1}>Vdc/4, *i*a <0, discharging	V_{CA2}<Vdc/8, *i*a<0, charging
	0	0	0	1	0	0	V_{CA1}<or>Vdc/4,*i*a>0,status quo	V_{CA2}<Vdc/8, *i*a >0, charging
	0	0	0	1	0	0	V_{CA1}<or>Vdc/4,*i*a<0, status quo	V_{CA2}>Vdc/8, *i*a <0, discharging

- **The current from A to A' is assumed to be the positive direction of current. Similar methods are used for generation of -Vdc/8 in other two phases.**

Generation of –2Vdc/8 and effects on capacitors in phase-A

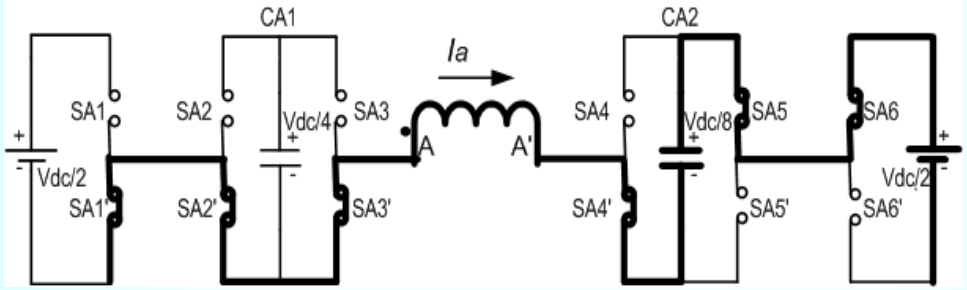


→ **CA1 discharges CA2 unaffected**

→ **CA1 charges CA2 unaffected**

The current from A to A' is assumed to be the positive direction of current

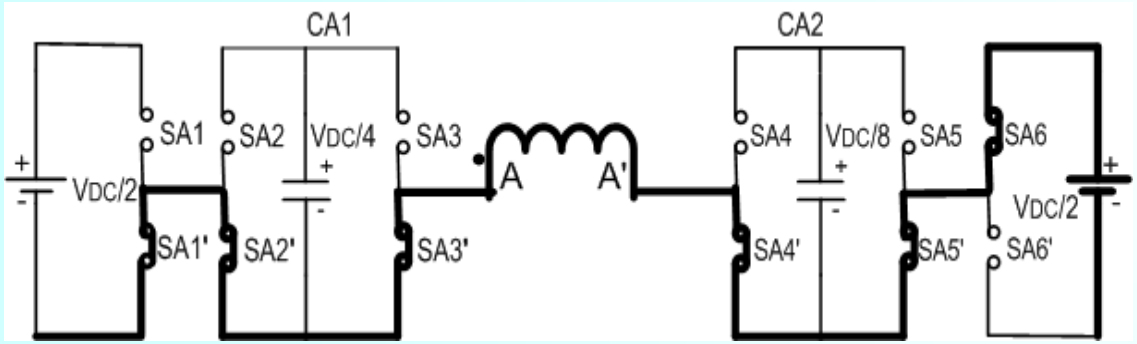
Switch-states for generation of –3Vdc/8



VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA 1	SA 2	SA 3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
-3Vdc/8	0	0	0	0	1	1	V_{CA1}<or>Vdc/4,*ia*>0,status quo	V_{CA2}>Vdc/8, *ia*>0, discharging
	0	0	0	0	1	1	V_{CA1}<or>Vdc/4,*ia*<0,status quo	V_{CA2}<Vdc/8, *ia*<0, charging
	0	1	0	1	0	0	V_{CA1}<Vdc/4, *ia* >0, charging	V_{CA2}<Vdc/8, *ia* >0, charging
	0	1	0	1	0	0	V_{CA1}>Vdc/4, *ia* <0, discharging	V_{CA2}>Vdc/8, *ia* <0, discharging
	0	0	1	1	0	1	V_{CA1}>Vdc/4, *ia* >0, discharging	V_{CA2}<Vdc/8, *ia* >0, charging
	0	0	1	1	0	1	V_{CA1}<Vdc/4, *ia* <0, charging	V_{CA2}>Vdc/8, *ia* <0, discharging

- **The current from A to A' is assumed to be the positive direction of current. Similar methods are used for generation of -3Vdc/8 in other two phases.**

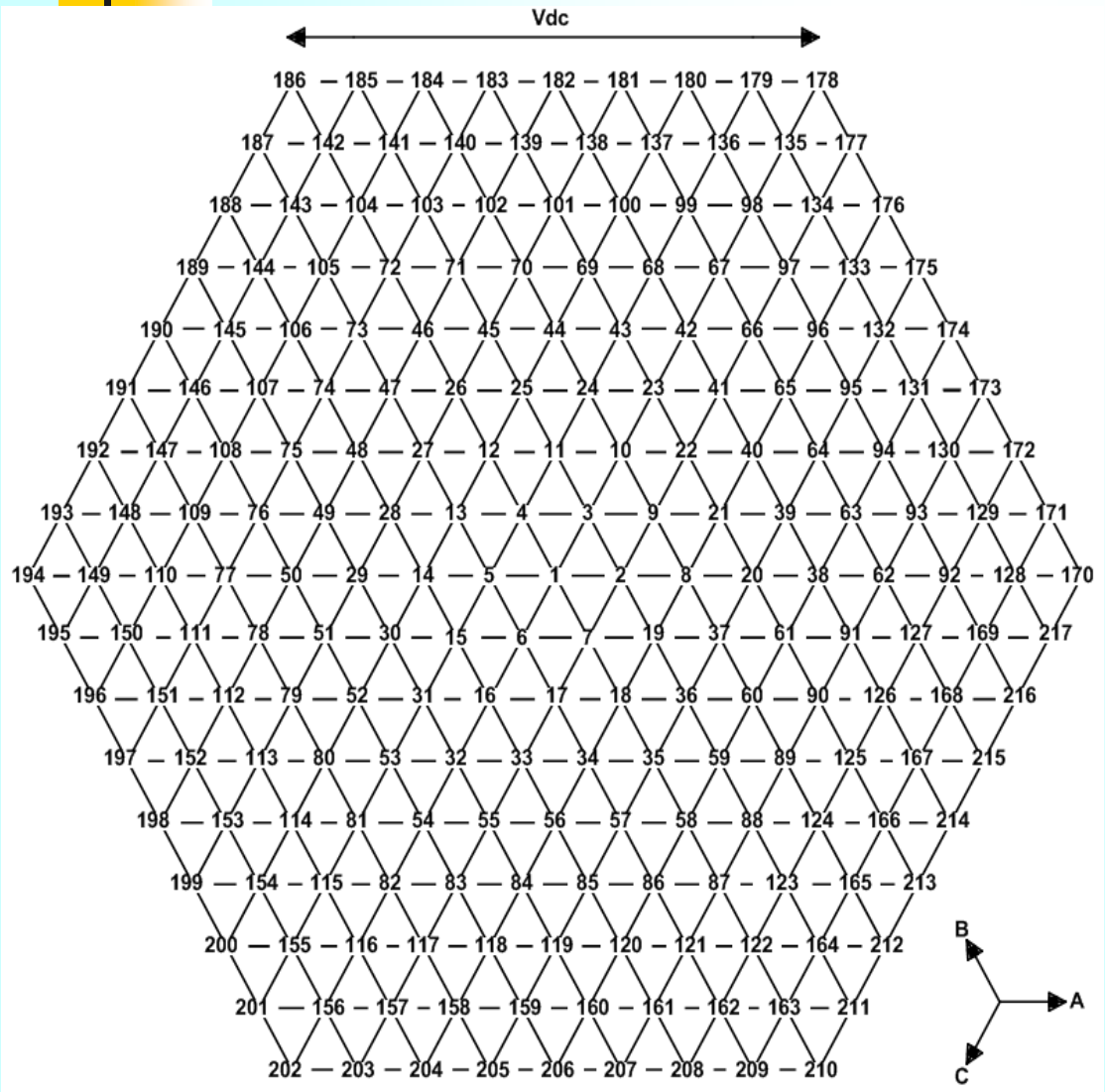
Generation of –Vdc/2



PHASE VOLTAGE LEVEL	SWITCH STATES						CONDITIONS FOR SWITCH STATE SELECTION	
	SA1	SA2	SA3	SA4	SA5	SA6	STATUS OF CA1	STATUS OF CA2
-Vdc/2	0	0	0	0	0	1	Unaffected	Unaffected
	0	1	1	1	1	1	Unaffected	Unaffected
	0	1	1	0	0	1	Unaffected	Unaffected
	0	0	0	1	1	1	Unaffected	Unaffected

The capacitor-voltages are not affected.

Nine-level Voltage Space Vector diagram



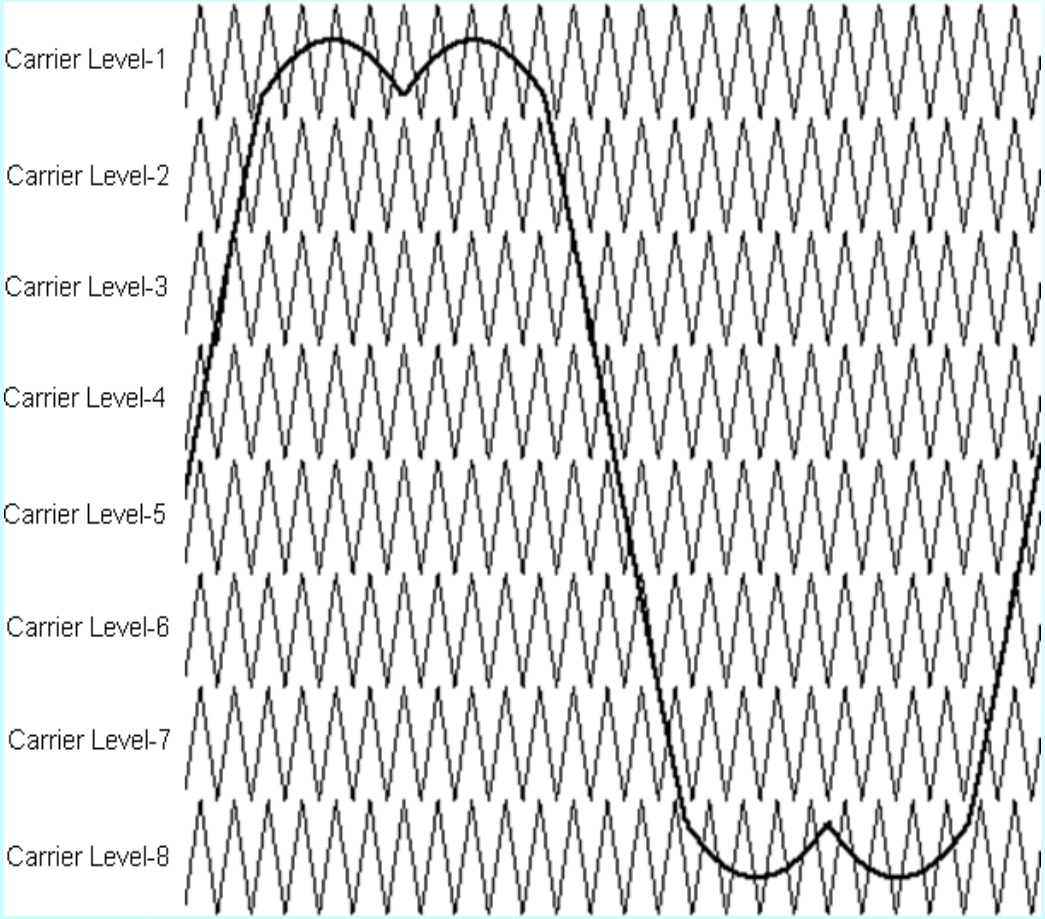
There are:

217 space vector locations.

729 inverter switching states.

Eight concentric hexagons.

Reference voltage waveform (after addition of V offset) and eight level shifted triangular carrier waveforms

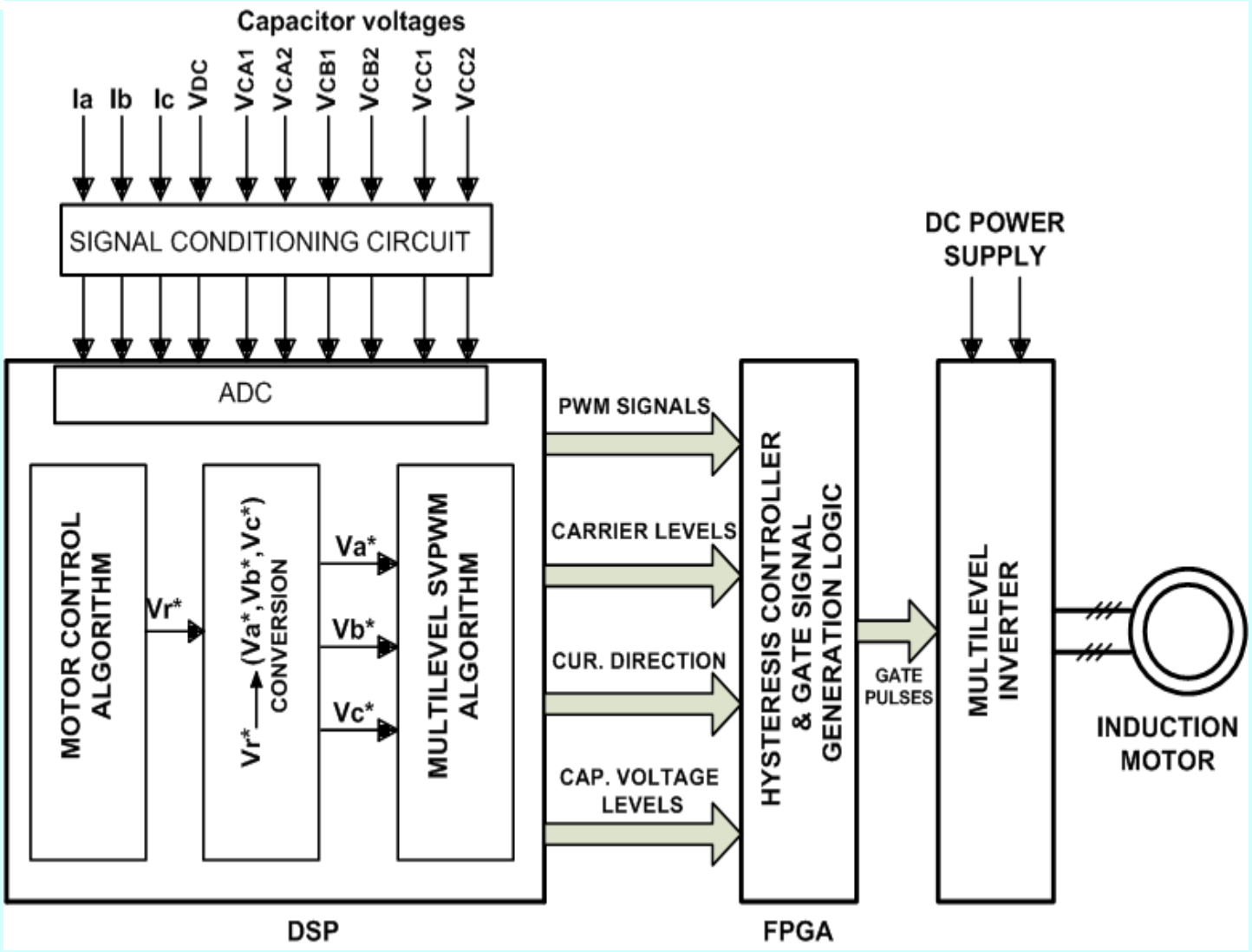


Modulation Index is defined as M = |Vs|/ Vdc

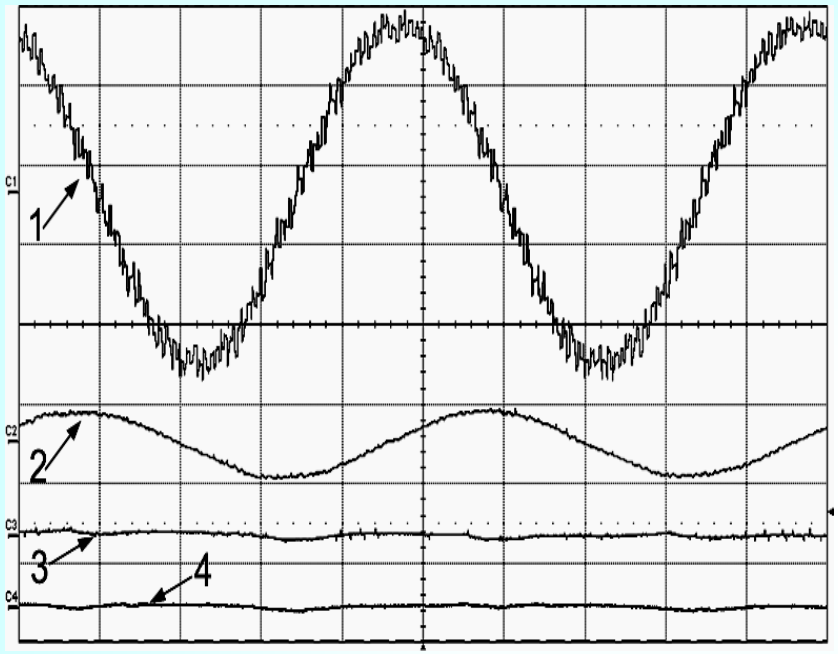
The reference voltage for M=0.8 spans all the eight level shifted triangular carriers.

This reference voltage waveform is compared with the level-shifted triangular carrier waveforms to generate the PWM signals.

Schematic diagram of the experimental set-up.



Experimental results for 9-level operation



[X-axis: 5ms/div]

1. Phase voltage
   [Y-axis: 100V/div]

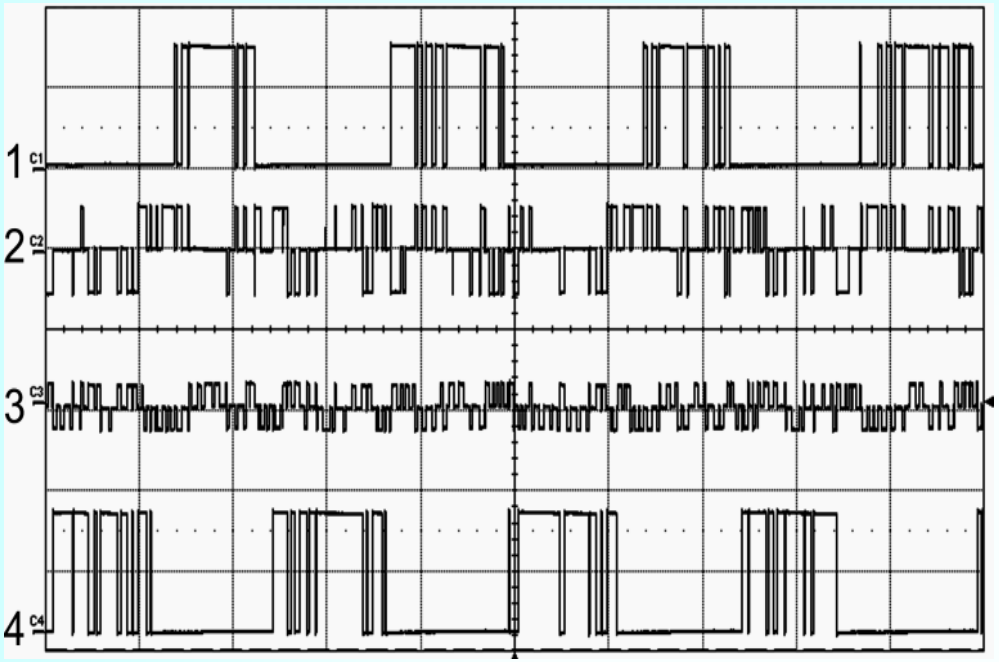
2. Phase current
   [Y-axis: 4A/div]

3. Capacitor-CA1 voltage ripple. [5V/div]

4. Capacitor-CA2 voltage ripple. [5V/div]

- The Inverter is operating in five-level mode (M=0.8)
- 40Hz operation of the motor.
- The capacitor peak to peak voltage ripple is less than 2V

Pole voltage waveforms for 9-level operation



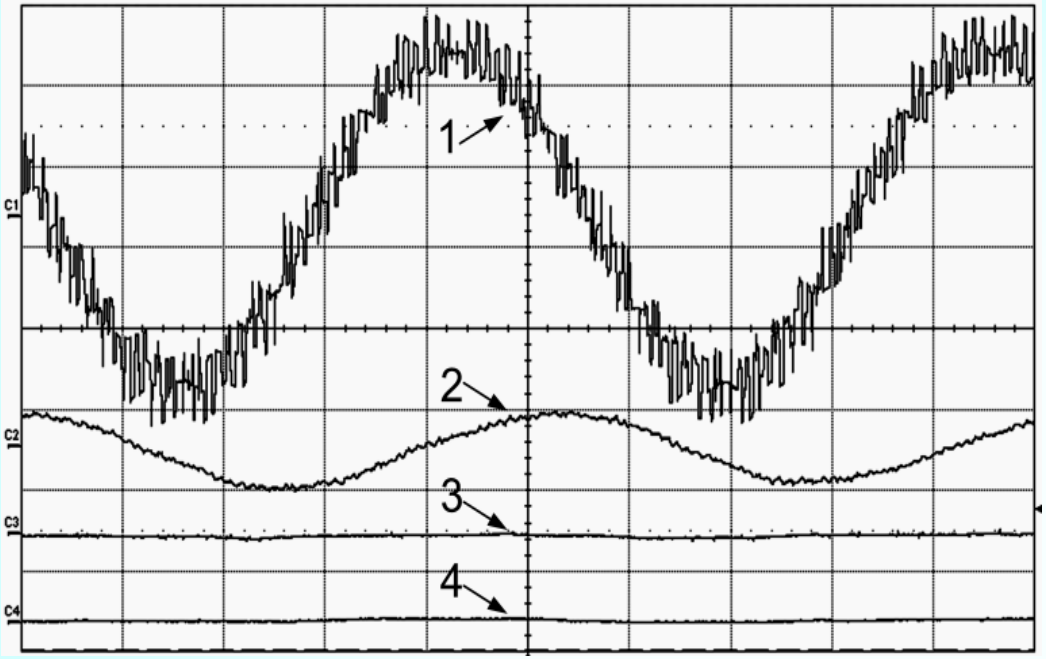
1. 2-level Inverter-1
2. H-bridge cell CA1
3. 2-level Inverter-2
4. H-bridge cell CA2

X-axis: 10ms/div

Y-axis: 100V/div

- High voltage inverters (i.e. 2-level inverter-1 and 2-level inverter-2) are switching only for half of the period in a fundamental cycle.

Experimental results for 5-level operation (M=0.36)

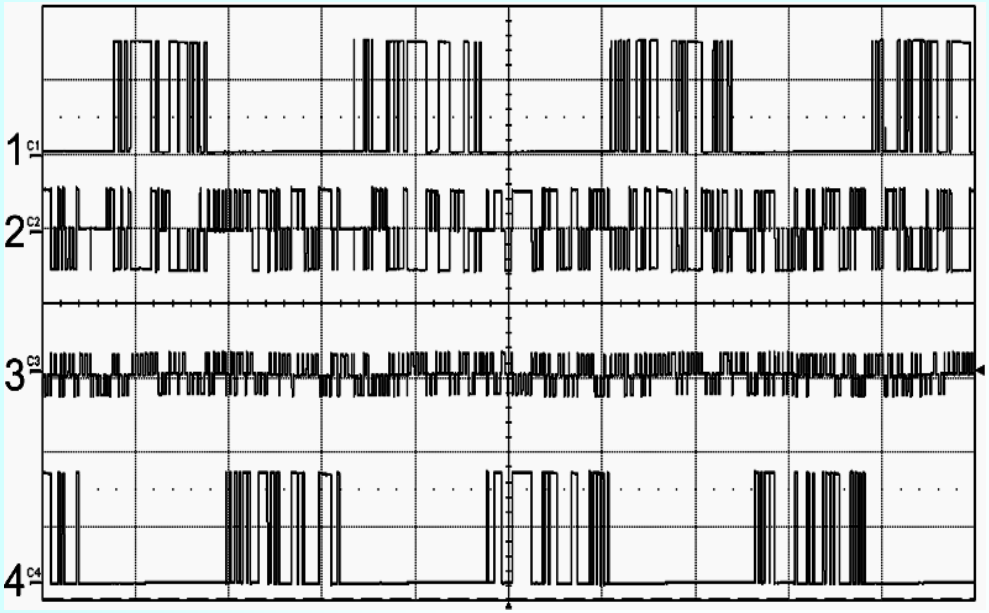


[X-axis: 10ms/div]

1. Phase voltage [Y-axis: 30V/div]
2. Phase current [Y-axis: 2A/div]
3. Capacitor-CA1 voltage ripple. [5V/div]
4. Capacitor-CA2 voltage ripple. [5V/div]

- Five-level operation of the Inverter (M=0.36)
- 18Hz operation of the motor.
- The capacitor peak-to-peak voltage ripple is less than 2V

Pole Voltage waveforms for 5-level operation (M=0.36)



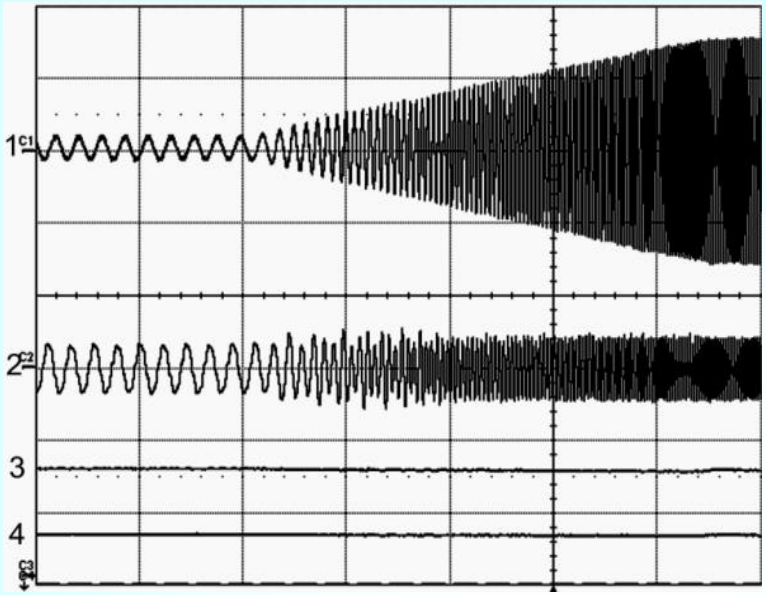
1. 2-level Inverter-1
2. H-bridge cell CA1
3. 2-level Inverter-2
4. H-bridge cell CA2

X-axis: 20ms/div

Y-axis: 100V/div

- High voltage fed inverters (i.e. 2-level inverter-1 and 2-level inverter-2) are switching only for half of the period in fundamental cycle
- Results in reduction in switching loss and improvement in efficiency of the drive.

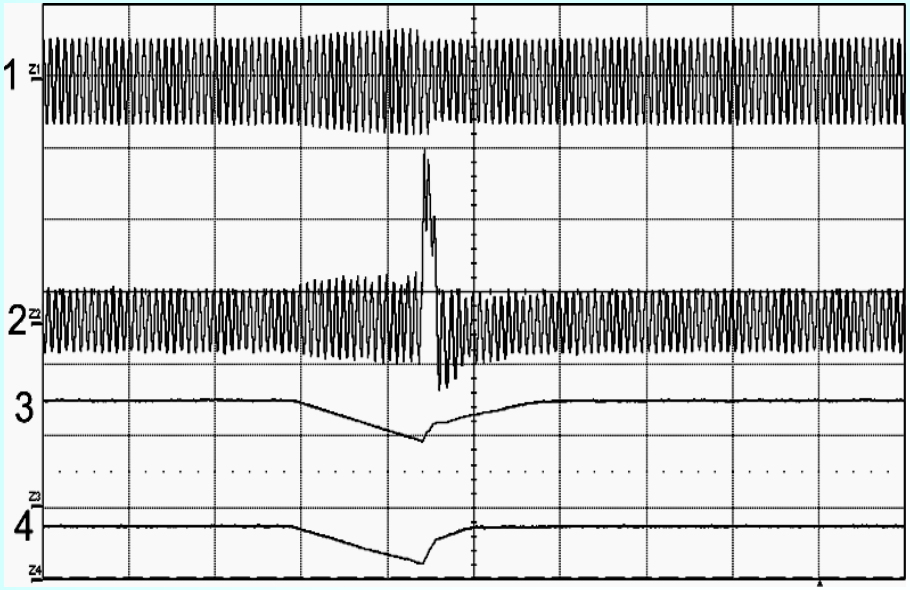
Transient performance



1. Phase voltage
   [Y-axis: 100V/div]
2. Phase current
   [Y-axis: 4A/div]
3. Capacitor-CA1 voltage
   [100V/div]
4. Capacitor-CA2 voltage
   [100V/div]

- Transient performance during acceleration of the drive
- Even though the accelerating the motor draws current much more than the steady state operation, the capacitor voltage is balanced for the full modulation range.
- Smooth transition from 4.5 Hz to 40 Hz operation corresponding to transition from two-level to nine-level operation.

Testing of capacitor voltage balancing algorithm



1. Phase voltage [Y-axis: 100V/div]
2. Phase current [Y-axis: 4A/div]
3. Capacitor-CA1 voltage [50V/div]
4. Capacitor-CA2 voltage [50V/div]

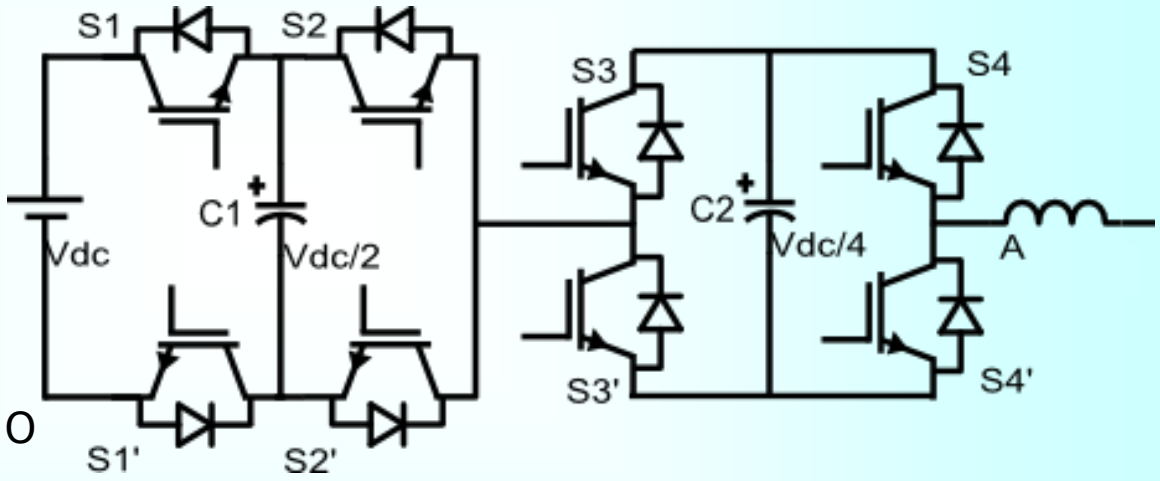
X-axis : 150ms/div

Effects on Voltage and Current waveforms when the capacitor voltage balancing scheme is momentarily disabled in all the phases.

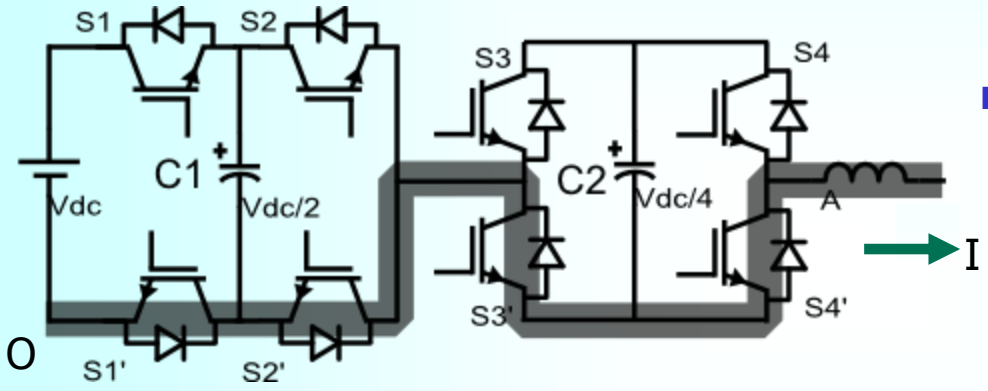
A five-level inverter with single DC source for AC drives with open-end stator winding

Five-Level Inverter Circuit Diagram

- Possible voltage levels.
  - 0
  - Vdc/4
  - Vdc/2
  - 3Vdc/4
  - Vdc

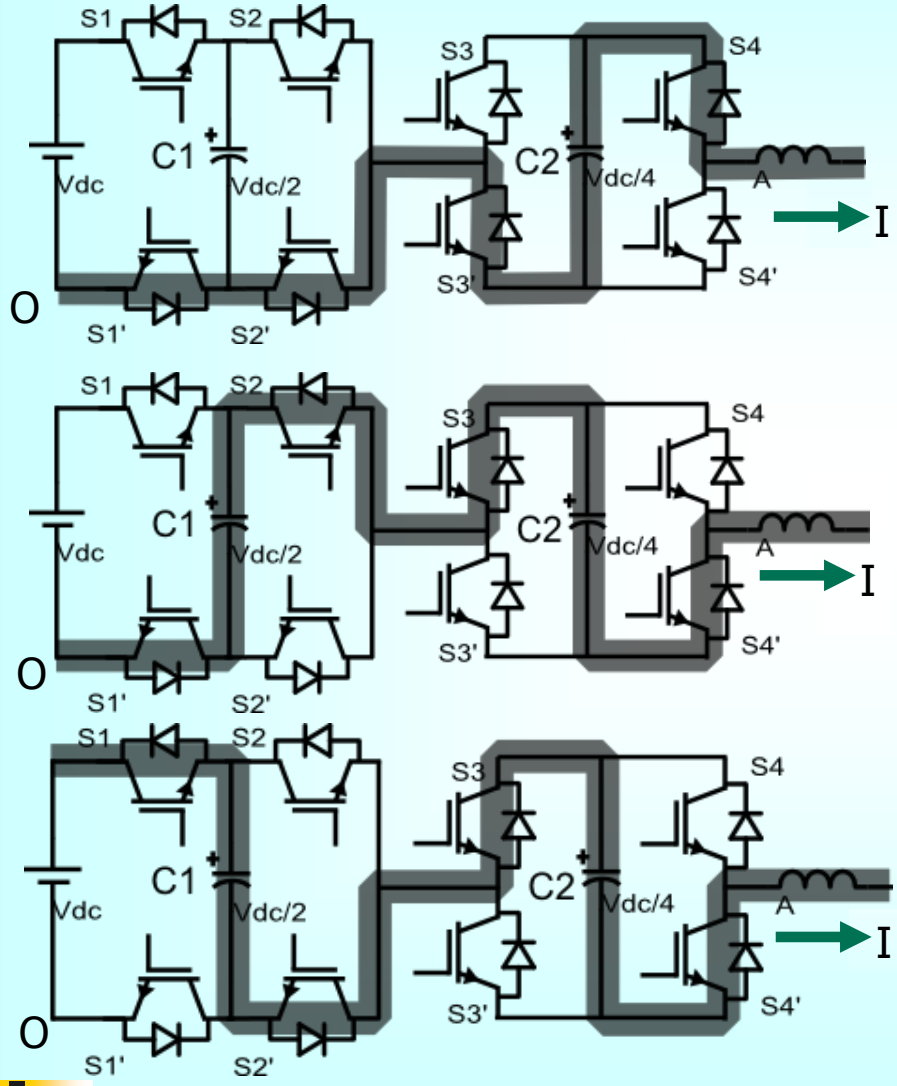


State for Voltage Level 0



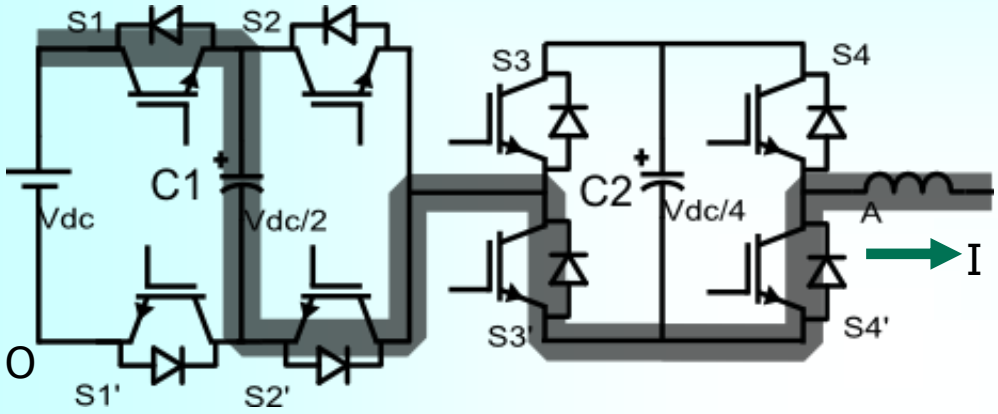
- State (0, 0, 0, 0)
  - C1 : No effect
  - C2 : No effect

Redundant States for Pole Voltage of Vdc/4 (+ve Current)

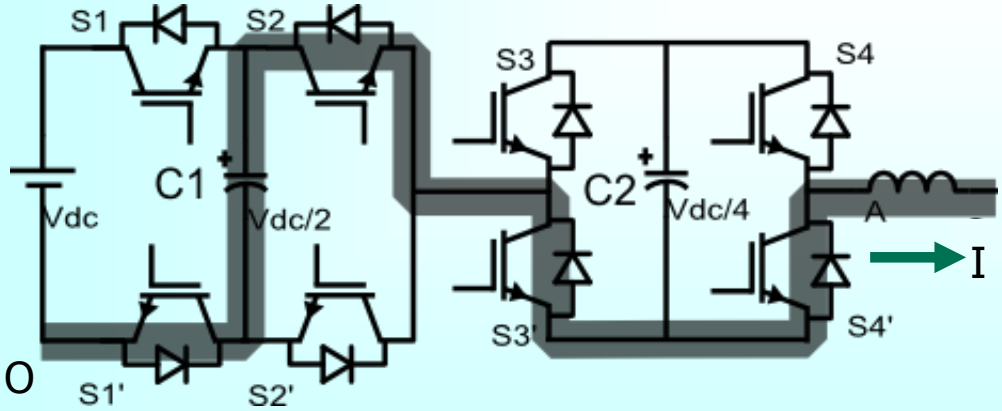


- State (0, 0, 0, 1)
  - C1 : No effect
  - C2 : Discharge
- State (0, 1, 1, 0)
  - C1 : Discharge
  - C2 : Charge
- State (1, 0, 1, 0)
  - C1 : Charge
  - C2 : Charge

Redundant States for Pole Voltage of Vdc/2 (+ve Current)

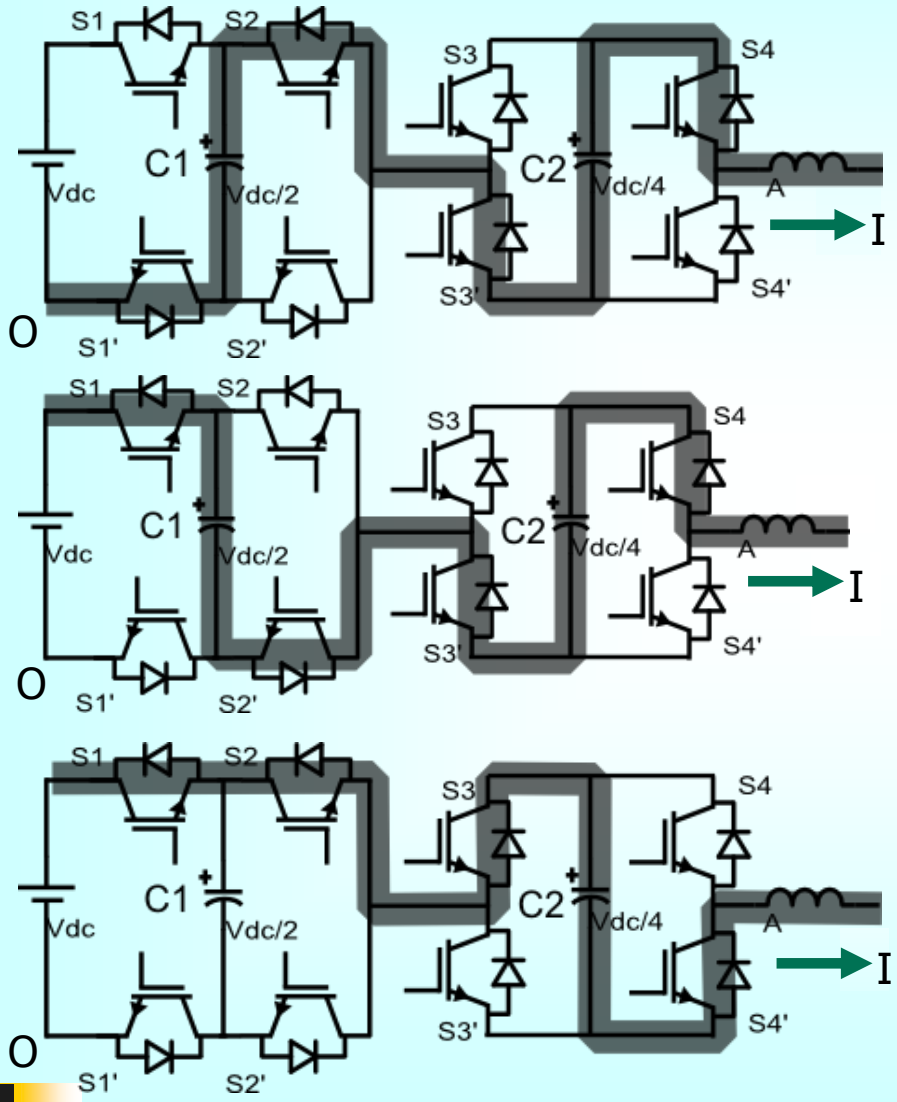


- State (1, 0, 0, 0)
  - C1 : Charge
  - C2 : No effect



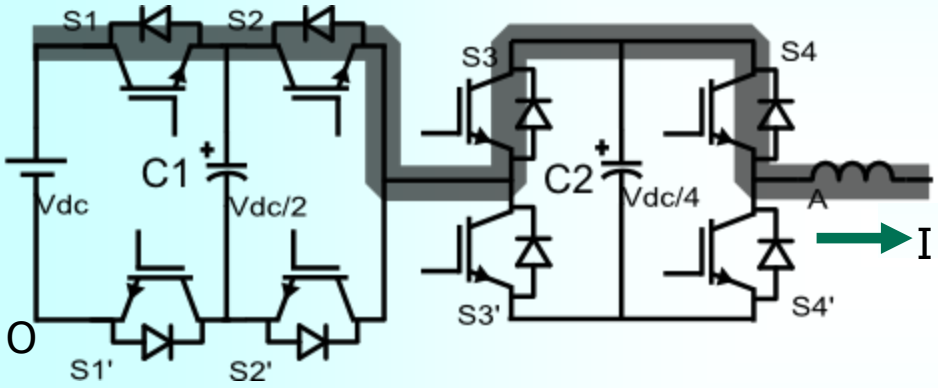
- State (0, 1, 0, 0)
  - C1 : Discharge
  - C2 : No effect

Redundant States for Pole Voltage of 3Vdc/4 (+ve Current)



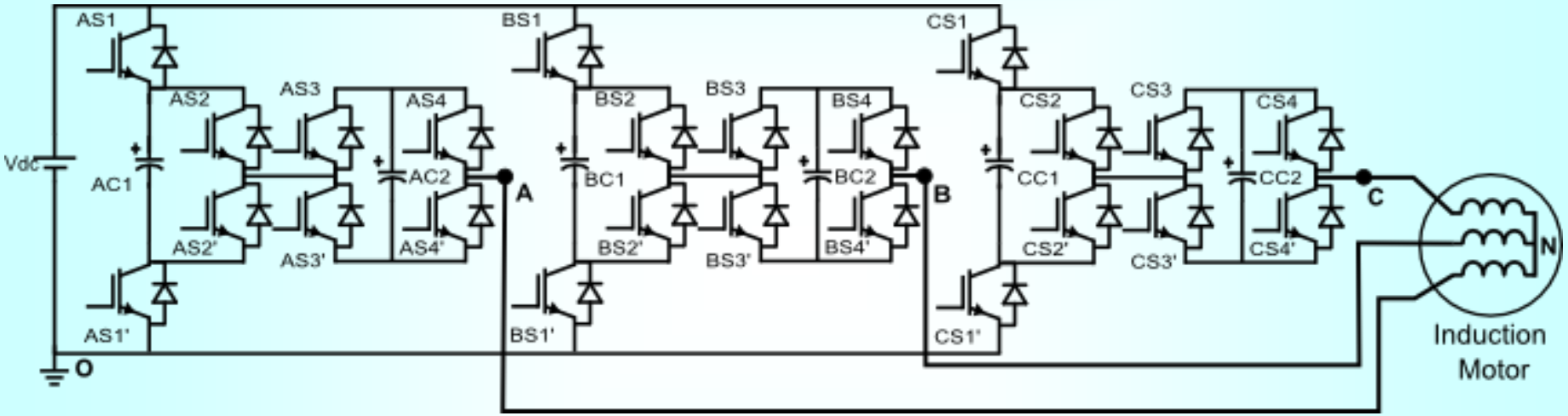
- State (0, 1, 0, 1)
  - C1 : Discharge
  - C2 : Discharge
- State (1, 0, 0, 1)
  - C1 : Charge
  - C2 : Discharge
- State (1, 1, 1, 0)
  - C1 : No Effect
  - C2 : Charge

State for Voltage Level Vdc

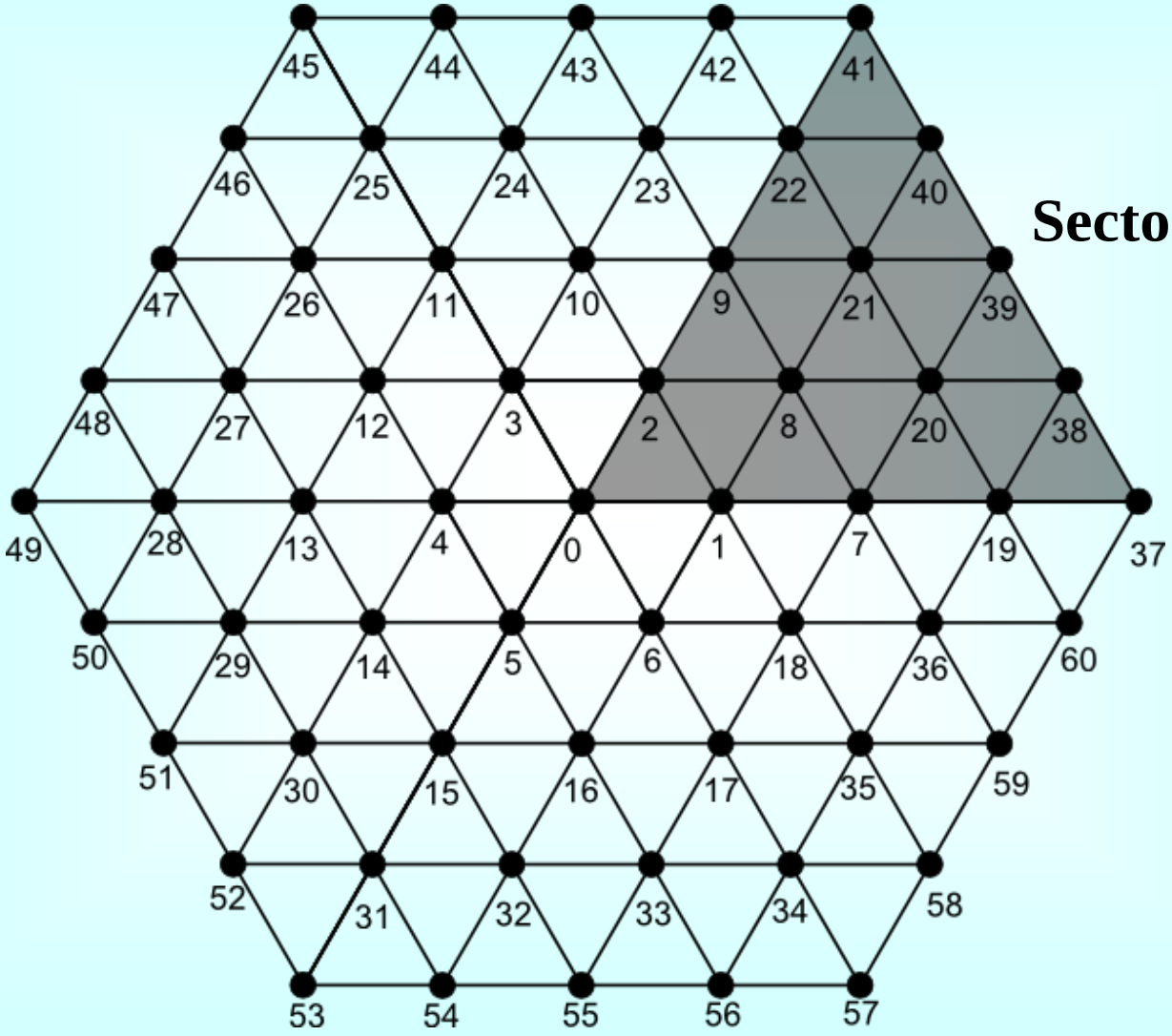


- State (1, 1, 1, 1)
  - C1 : No effect
  - C2 : No effect

Three Phase Circuit Diagram

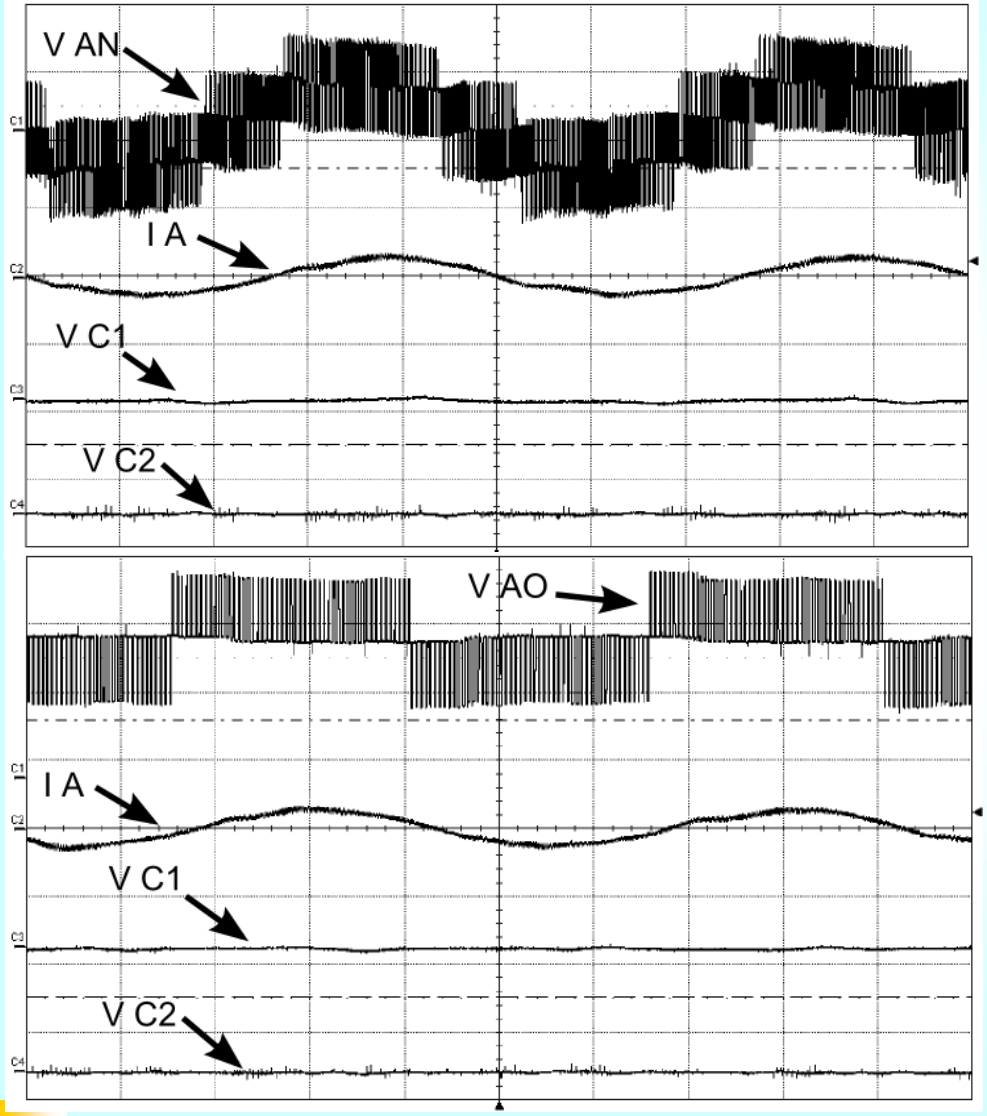


Five Level Three Phase Space Vector Polygon



Sector-I

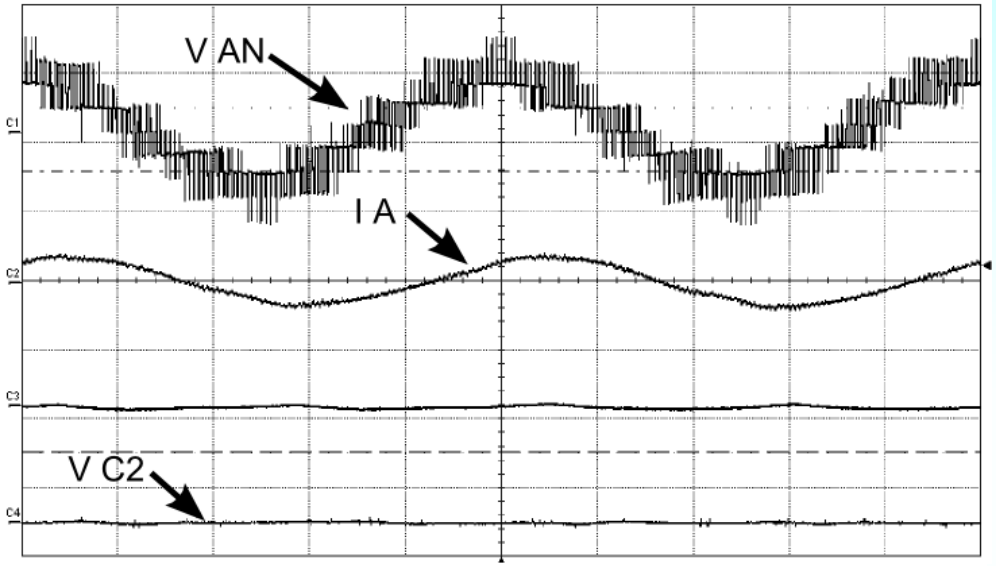
Phase and Pole Voltage for 10 Hz



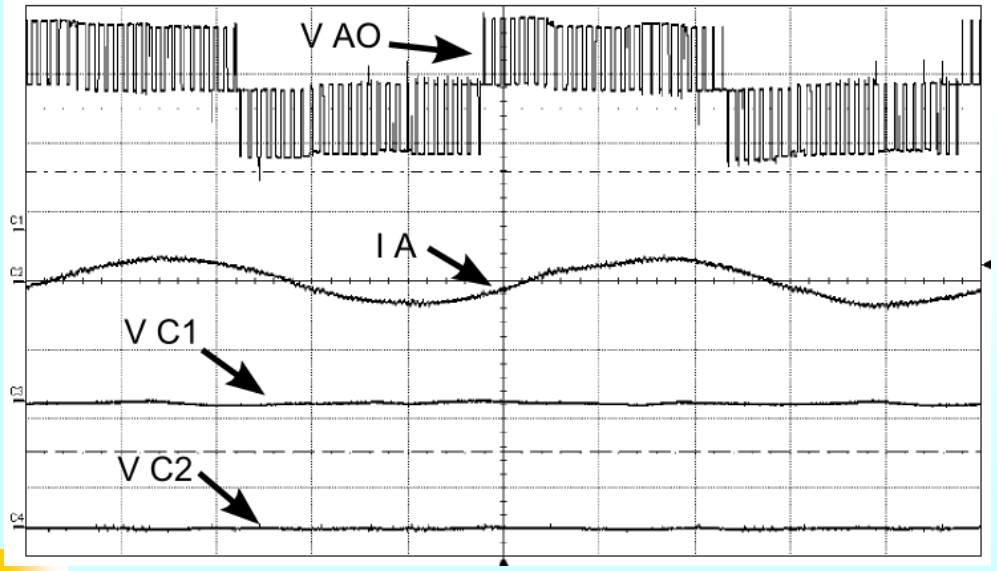
- V AN: Phase Voltage (50V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 20mS/div

- V A0: Pole Voltage (50V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 20mS/div

Phase and Pole Voltage for 20 Hz

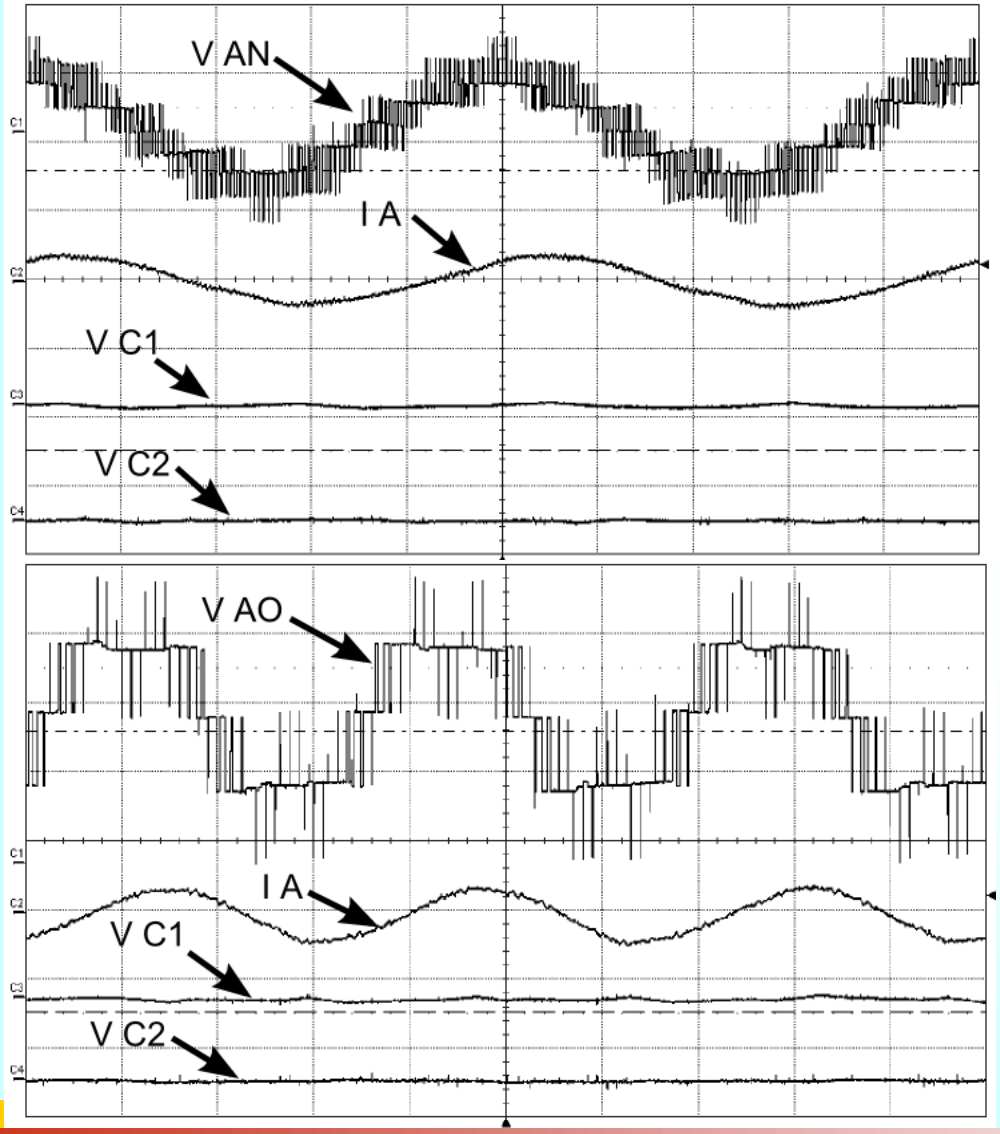


- V AN: Phase Voltage (100V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 10mS/div



- V A0: Pole Voltage (100V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 10mS/div

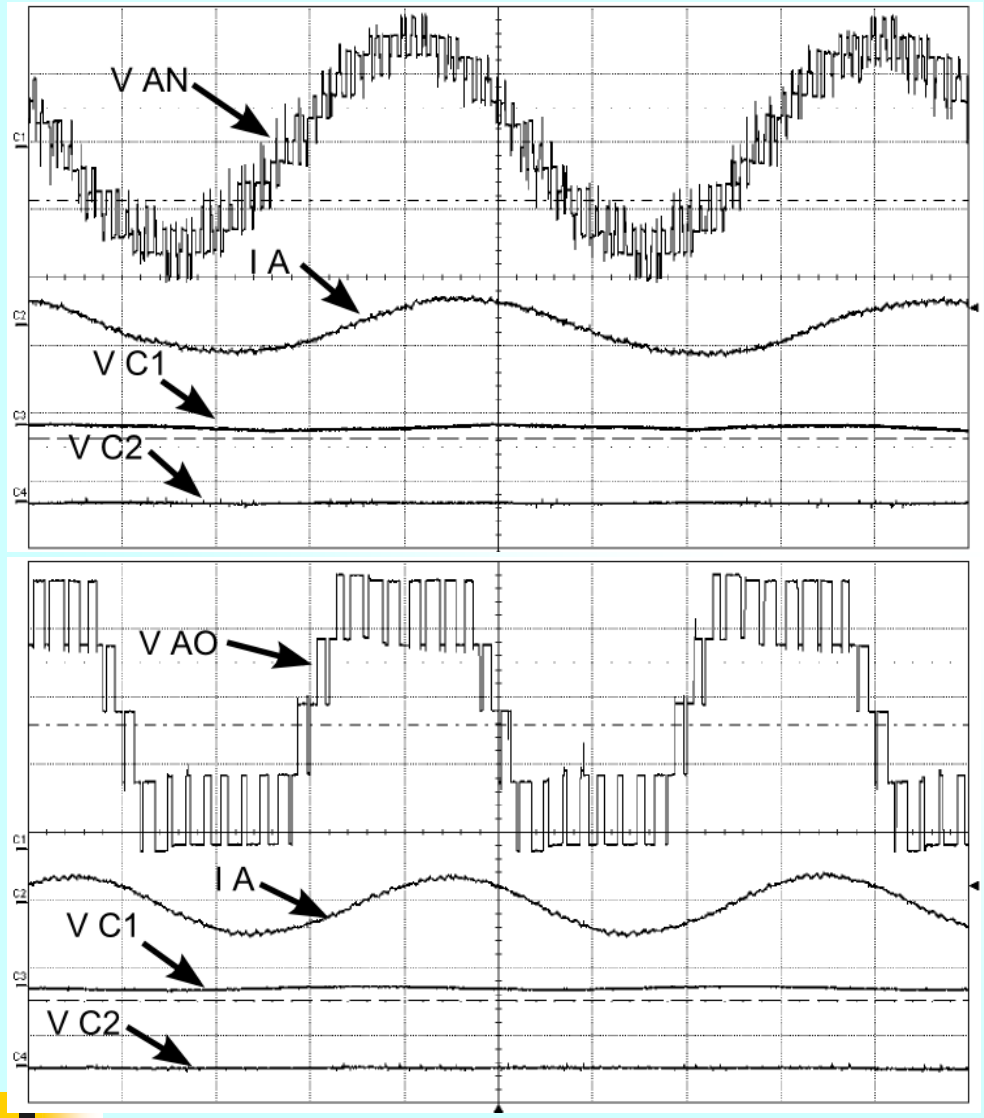
Phase and Pole Voltage for 30 Hz



- V AN: Phase Voltage (100V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 10mS/div

- V A0: Pole Voltage (100V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 10mS/div

Phase and Pole Voltage for 40 Hz

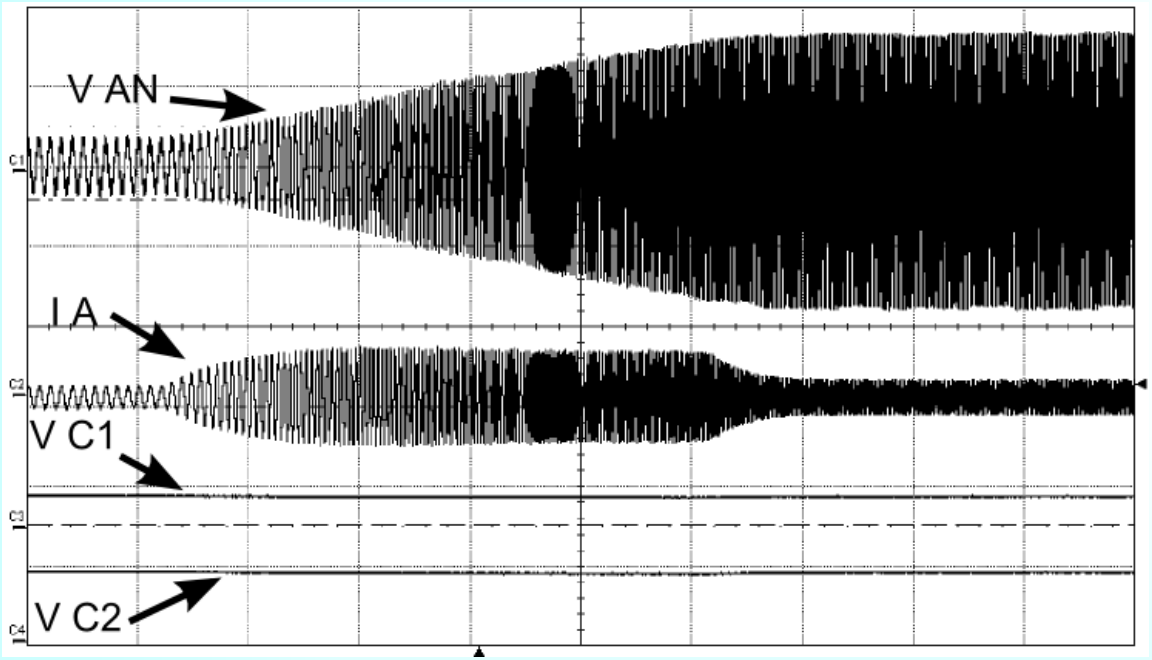


- V AN: Phase Voltage (100V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 5mS/div

- V A0: Pole Voltage (100V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 Voltage Ripple (5V/div)
- VC2: Cap2 Voltage Ripple (10V/div)
- Time scale: 5mS/div

Capacitor Voltage Under Sudden Acceleration

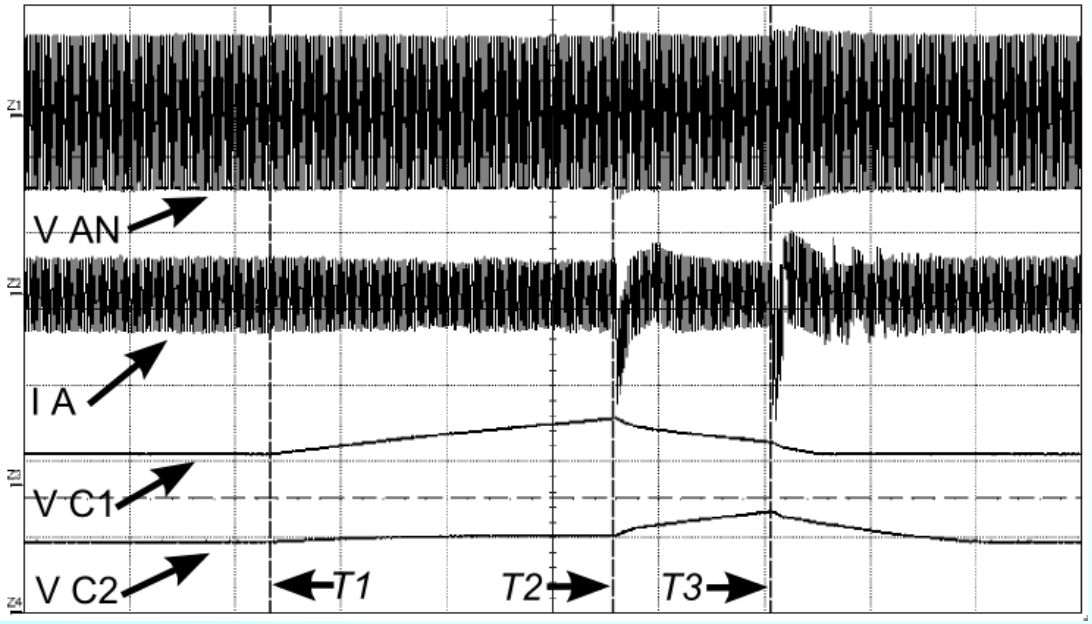
- The motor is accelerated from 10Hz to 40Hz at no load and the capacitor voltages are almost constant in this duration



- V AN: Phase Voltage (200V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 DC Voltage (200V/div)
- VC2: Cap2 DC Voltage (50V/div)
- Time scale: 1S/div

Capacitor Balancing Algorithm Test

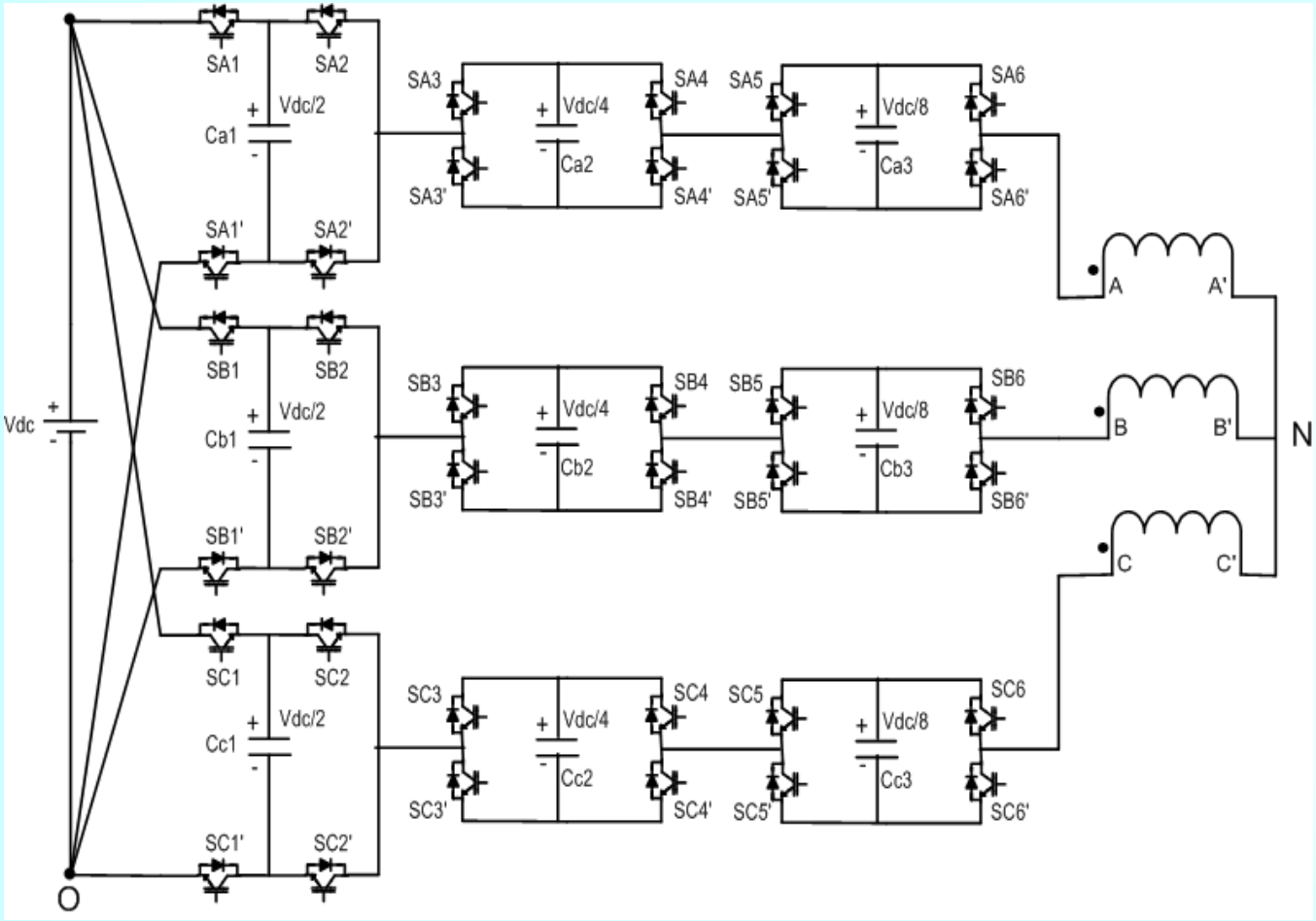
- The Capacitor balancing algorithm has been disabled for C1 and C2 at T1, enabled for C1 at T2 and C2 at T3.



- V AN: Phase Voltage (200V/div)
- IA : Phase Current (2A/div)
- VC1: Cap1 DC Voltage (200V/div)
- VC2: Cap2 DC Voltage (50V/div)
- Time scale: 2S/div

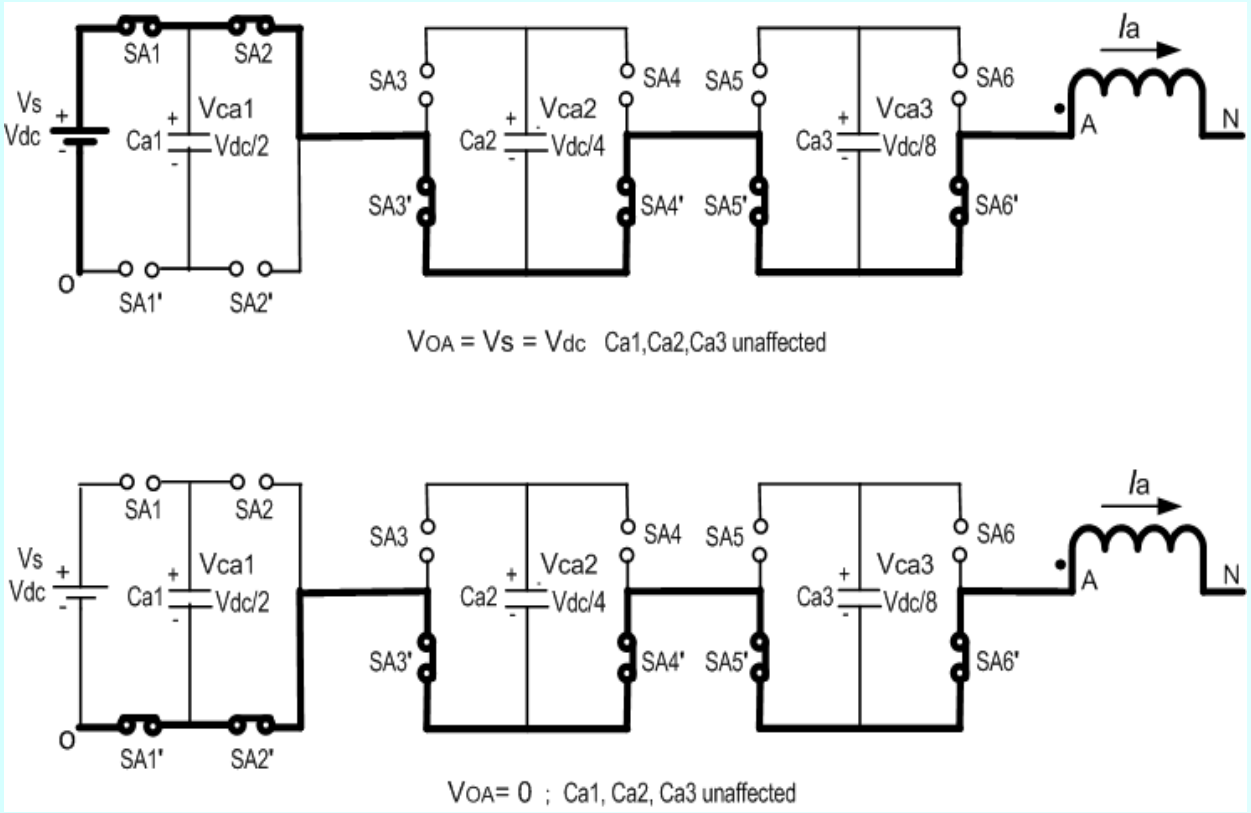
A reduced device-count hybrid multilevel inverter topology with single DC source and improved fault tolerance.

9-level version of the Proposed topology



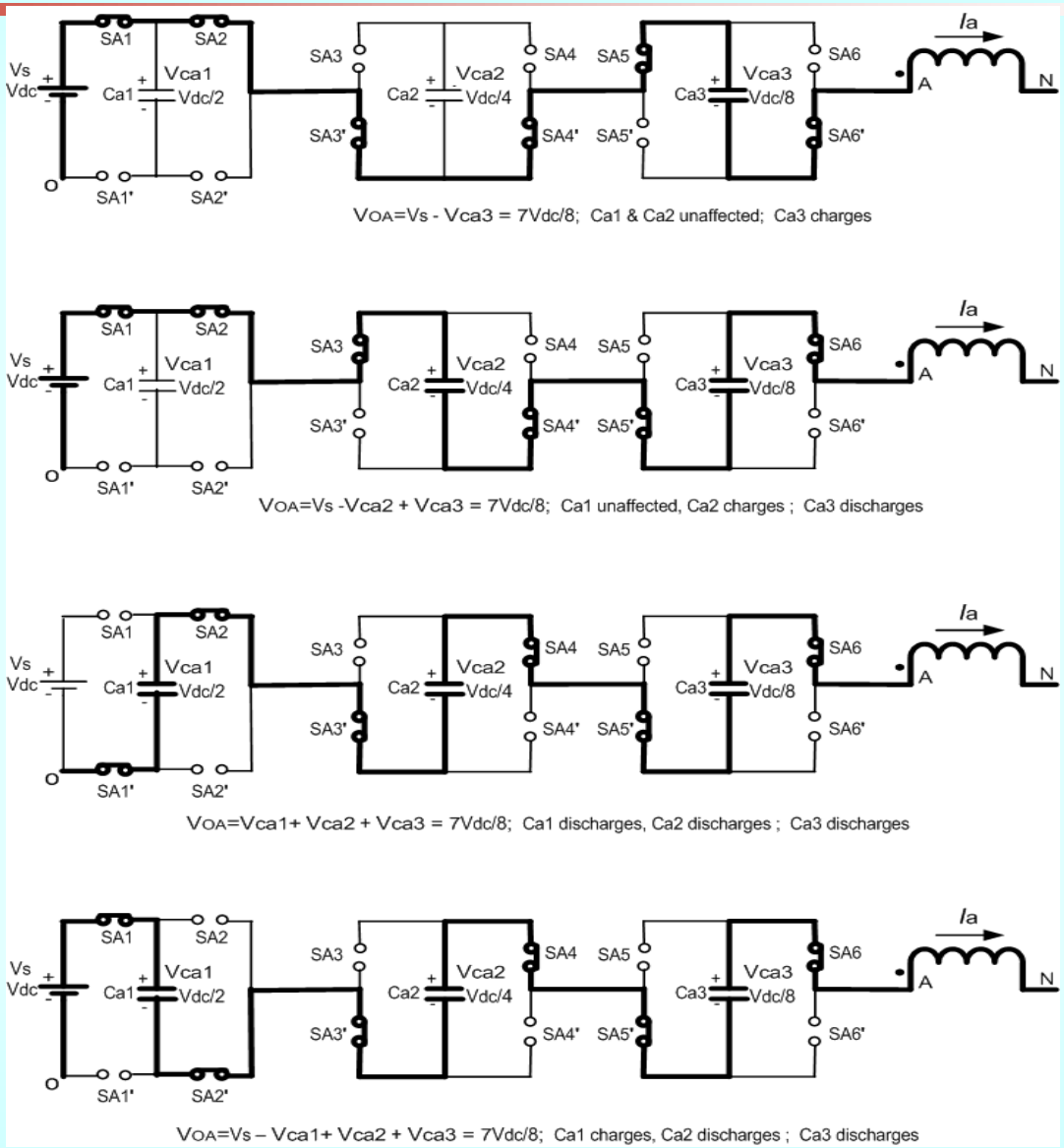
The nine pole voltage levels : V_{dc}, $7V_{dc}/8$, $6V_{dc}/8$, $5V_{dc}/8$, $4V_{dc}/8$, $3V_{dc}/8$, $2V_{dc}/8$, $V_{dc}/8$ 0 (with respect to the negative terminal of the DC source 'O')

Generation of Vdc and 0



Capacitor-voltages are not affected

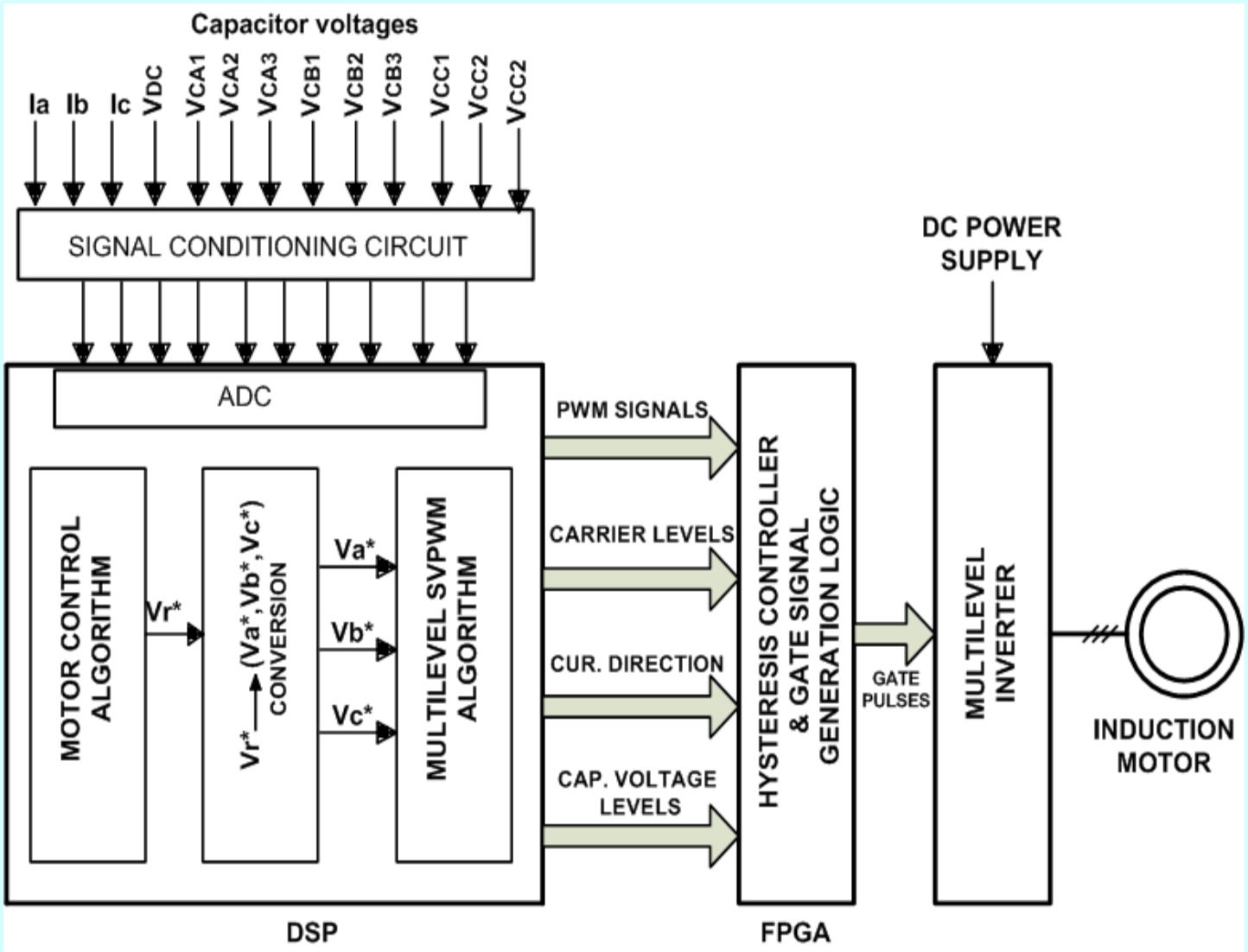
Generation of 7Vdc/8



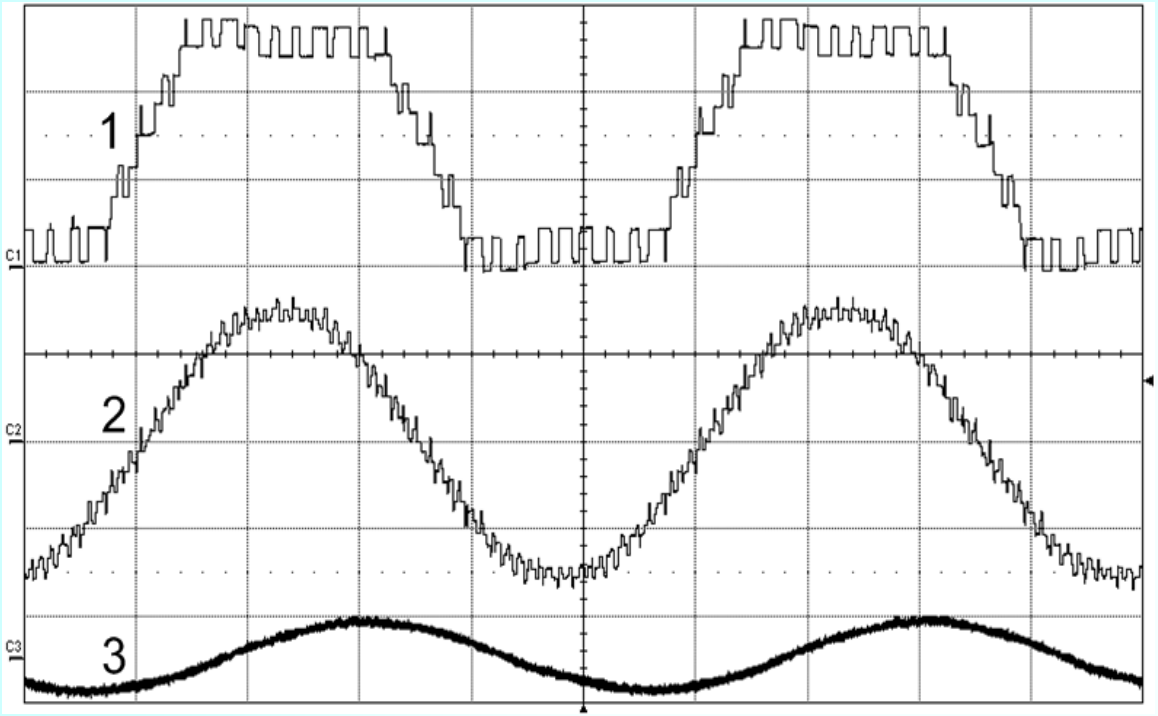
Switch states for generation of different voltage levels

Voltage Level	Method of Generation	Switch States						Effect on Capacitors when current is positive		
		SA1	SA2	SA3	SA4	SA5	SA6	Ca1	Ca2	Ca3
8Vdc/8	Vs = Vdc=8Vdc/8	1	1	0	0	0	0	No effect	No effect	No effect
7Vdc/8	Vs-Vca3	1	1	0	0	1	0	No effect	No effect	Charging
	Vs–Vca2+Vca3	1	1	1	0	0	1	No effect	Charging	Discharging
	Vs–Vca1+Vca2+Vca3	1	0	0	1	0	1	Charging	Discharging	Discharging
	Vca1+ Vca2+Vca3	0	1	0	1	0	1	Discharging	Discharging	Discharging
6Vdc/8	Vs–Vca2	1	1	1	0	0	0	No effect	Charging	No effect
	Vs–Vca1+ Vca2	1	0	0	1	0	0	Charging	Discharging	No effect
	Vca1+ Vca2	0	1	0	1	0	0	Discharging	Discharging	No effect
5Vdc/8	Vca1+ Vca2–Vca3	0	1	0	1	1	0	Discharging	Discharging	Charging
	Vca1+Vca3	0	1	0	0	0	1	Discharging	No effect	Discharging
	Vs–Vca1+Vca3	1	0	0	0	0	1	Charging	No effect	Discharging
	Vs–Vca2–Vca3	1	1	1	0	1	0	No effect	Charging	Charging
	Vs–Vca1+ Vca2–Vca3	1	0	0	1	1	0	Charging	Discharging	Charging
4Vdc/8	Vca1	0	1	0	0	0	0	Discharging	No effect	No effect
	Vs–Vca1	1	0	0	0	0	0	Charging	No effect	No effect
3Vdc/8	Vca1–Vca3	0	1	0	0	1	0	Discharging	No effect	Charging
	Vca2+Vca3	0	0	0	1	0	1	No effect	Discharging	Discharging
	Vca1– Vca2+Vca3	0	1	1	0	0	1	Discharging	Charging	Discharging
	Vs–Vca1– Vca2+Vca3	1	0	1	0	0	1	Charging	Charging	Discharging
	Vs–Vca1– Vca3	1	0	0	0	1	0	Charging	No effect	Charging
2Vdc/8	Vca2	0	0	0	1	0	0	No effect	Discharging	No effect
	Vca1– Vca2	0	1	1	0	0	0	Discharging	Charging	No effect
	Vs–Vca1– Vca2	1	0	1	0	0	0	Charging	Charging	No effect
Vdc/8	Vca3	0	0	0	0	0	1	No effect	No effect	Discharging
	Vca2–Vca3	0	0	0	1	1	0	No effect	Discharging	Charging
	Vca1– Vca2–Vca3	0	1	1	0	1	0	Discharging	Charging	Charging
	Vs–Vca1–Vca2–Vca3	1	0	1	0	1	0	Charging	Charging	Charging
0	0	0	0	0	0	0	0	No effect	No effect	No effect

Schematic diagram of the experimental setup



Experimental results – 9-level operation (40Hz)



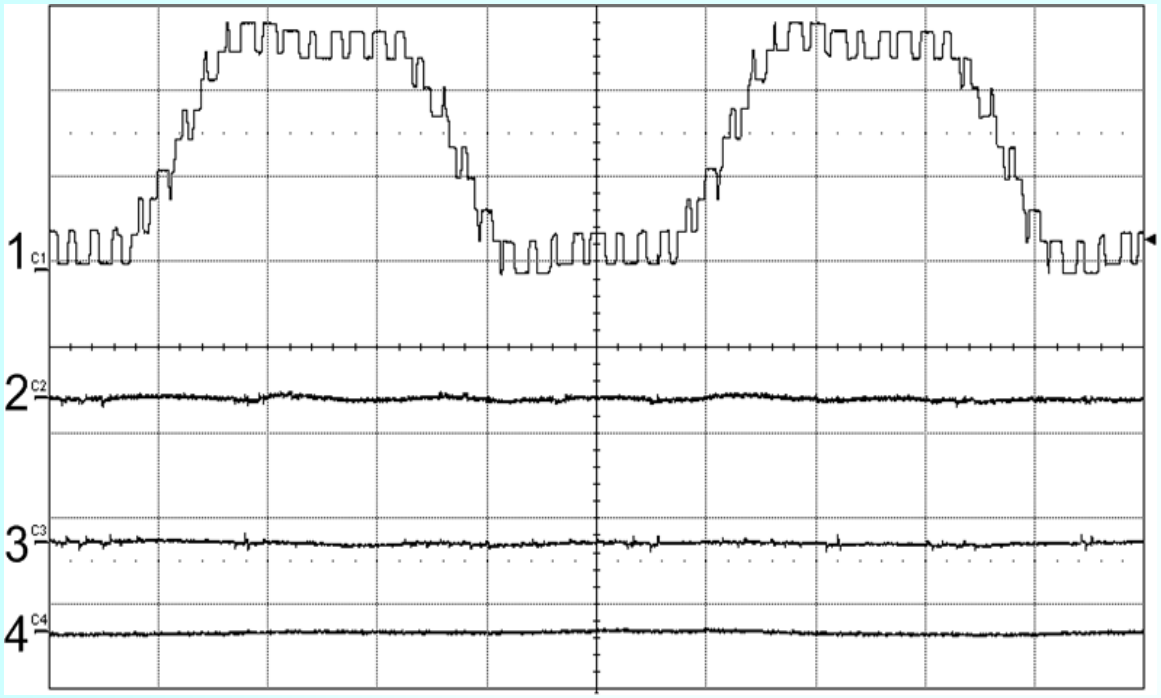
[X-axis: 5ms/div]

1. Pole voltage
   [Y-axis: 70V/div]

2. Phase voltage
   [Y-axis: 70V/div]

3. . Phase current
   [Y-axis: 2A/div]

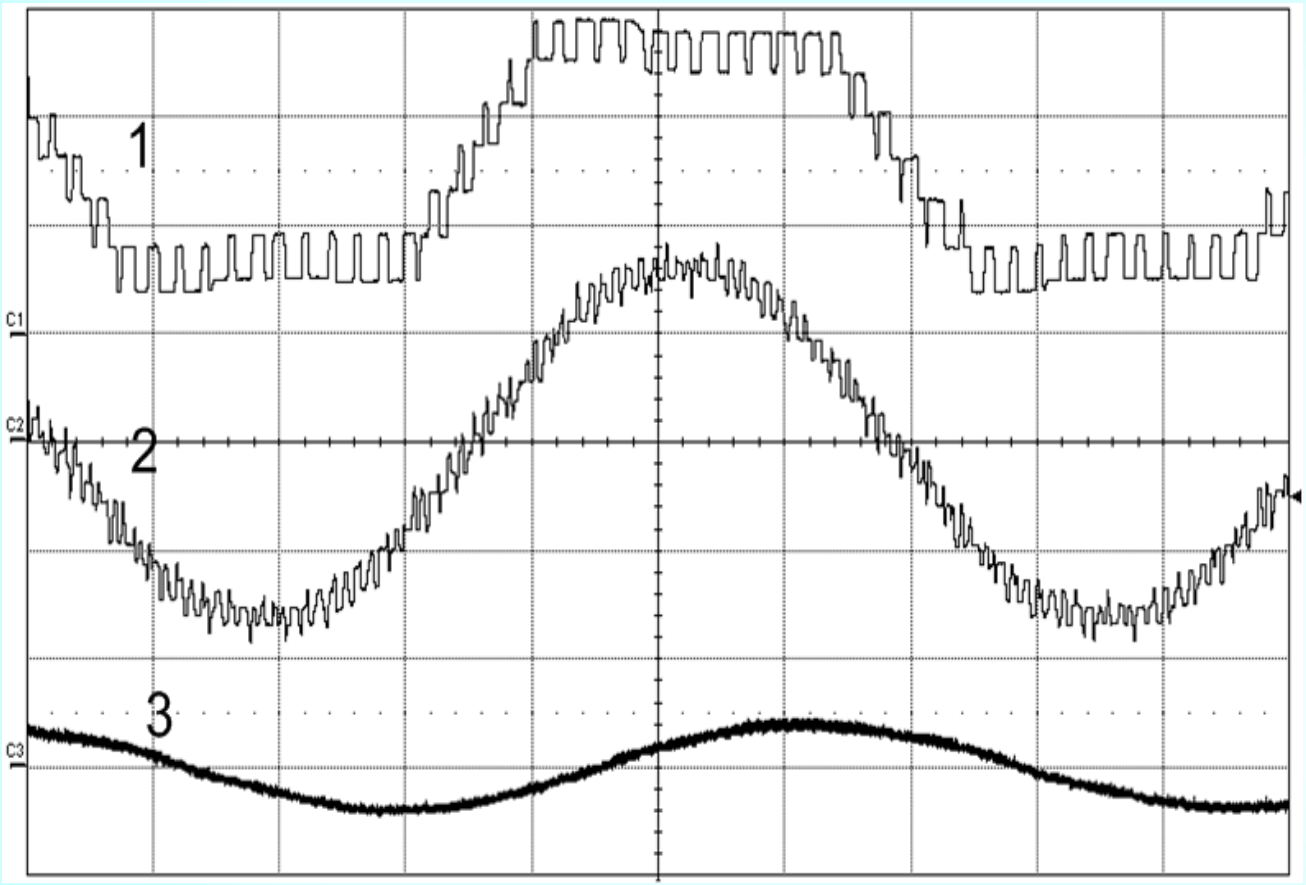
Experimental results – 9-level operation (40Hz)



[X-axis: 5ms/div]

1. Pole voltage [Y-axis: 70V/div]
2. Capacitor-CA1 voltage ripple. [10V/div]
3. Capacitor-CA2 voltage ripple. [10V/div]
4. Capacitor-CA3 voltage ripple. [10V/div]

Experimental results – 7-level operation (30Hz)



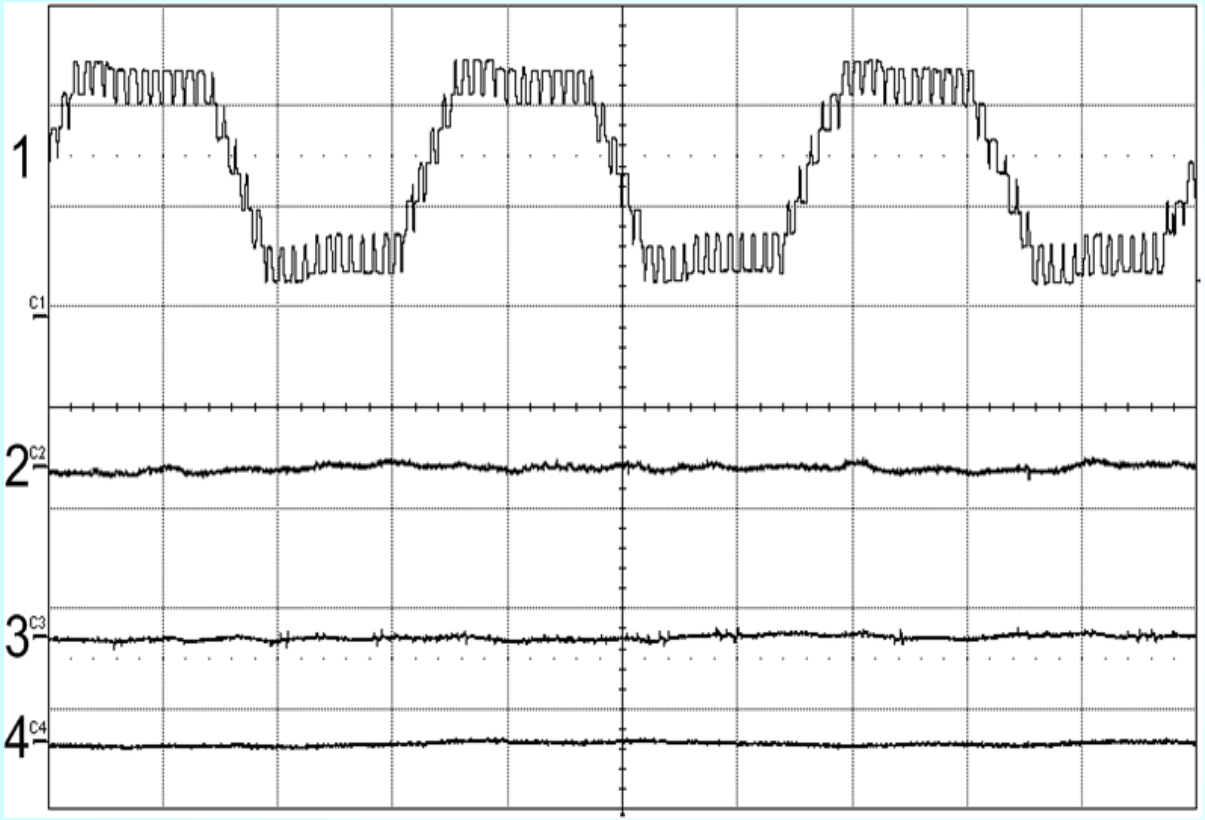
[X-axis: 5ms/div]

1. Pole voltage
   [Y-axis: 60V/div]

2. Phase voltage
   [Y-axis: 50V/div]

3. . Phase current
   [Y-axis: 2A/div]

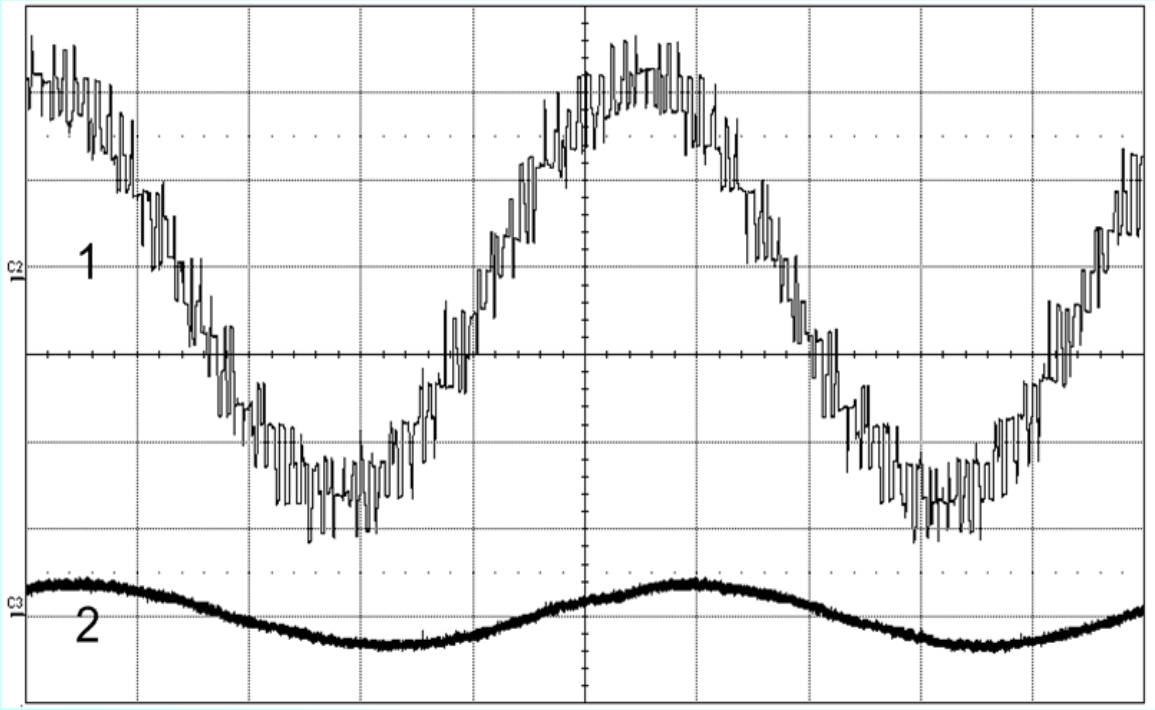
Experimental results – 7-level operation (30Hz)



[X-axis: 5ms/div]

1. Pole voltage [Y-axis: 70V/div]
2. Capacitor-CA1 voltage ripple. [10V/div]
3. Capacitor-CA2 voltage ripple. [10V/div]
4. Capacitor-CA3 voltage ripple. [10V/div]

Experimental results – 5-level operation (20Hz)

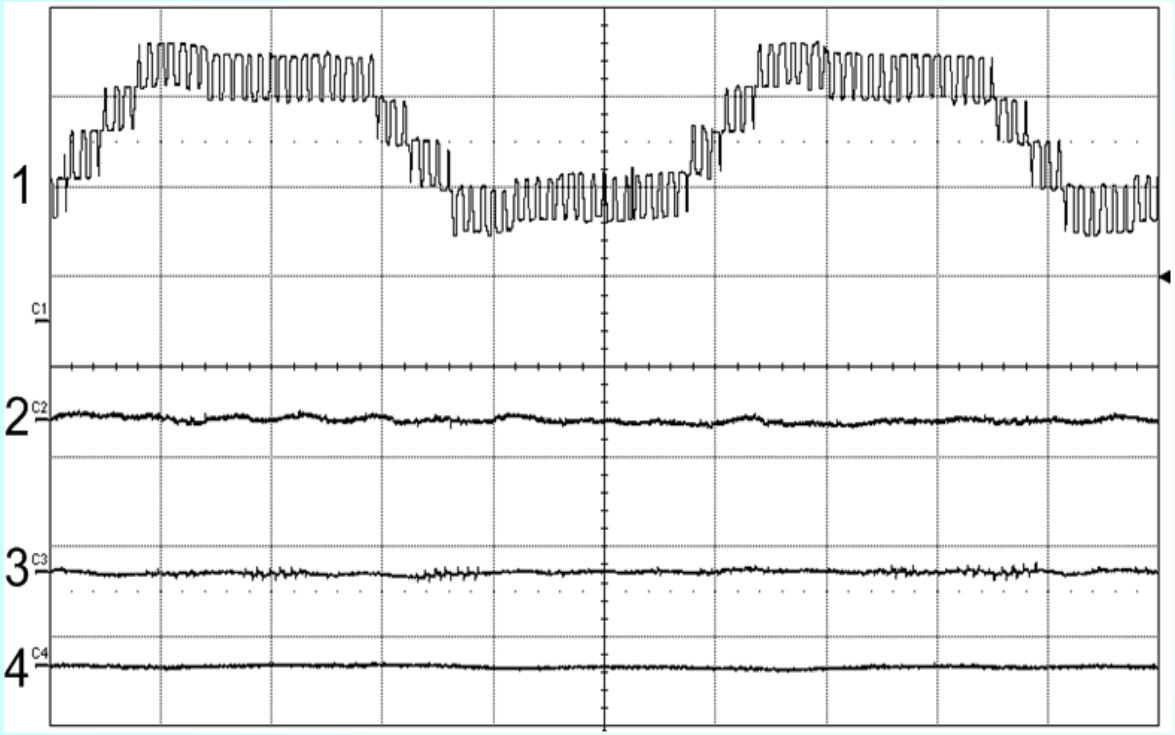


1. Phase voltage
   [Y-axis: 20V/div]

2. Phase current
   [Y-axis: 2A/div]

[X-axis: 10ms/div]

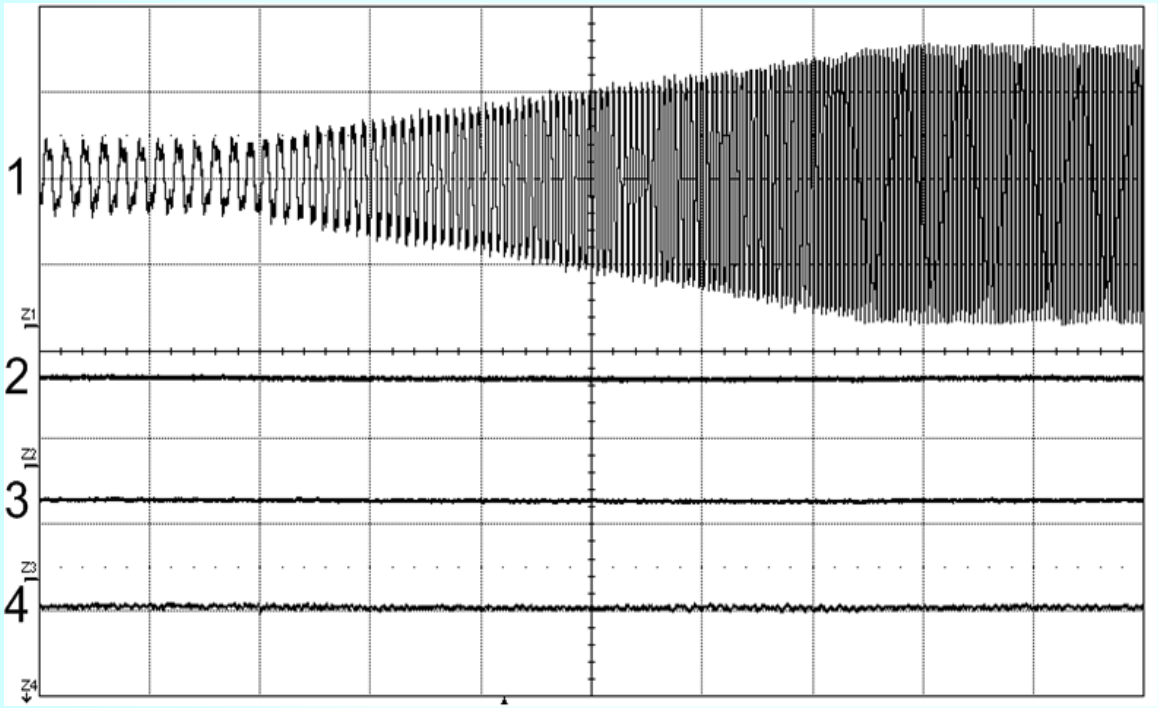
Experimental results – 5-level operation (20Hz)



[X-axis: 10ms/div]

1. Pole voltage [Y-axis: 50V/div]
2. Capacitor-CA1 voltage ripple. [10V/div]
3. Capacitor-CA2 voltage ripple. [10V/div]
4. Capacitor-CA3 voltage ripple. [10V/div]

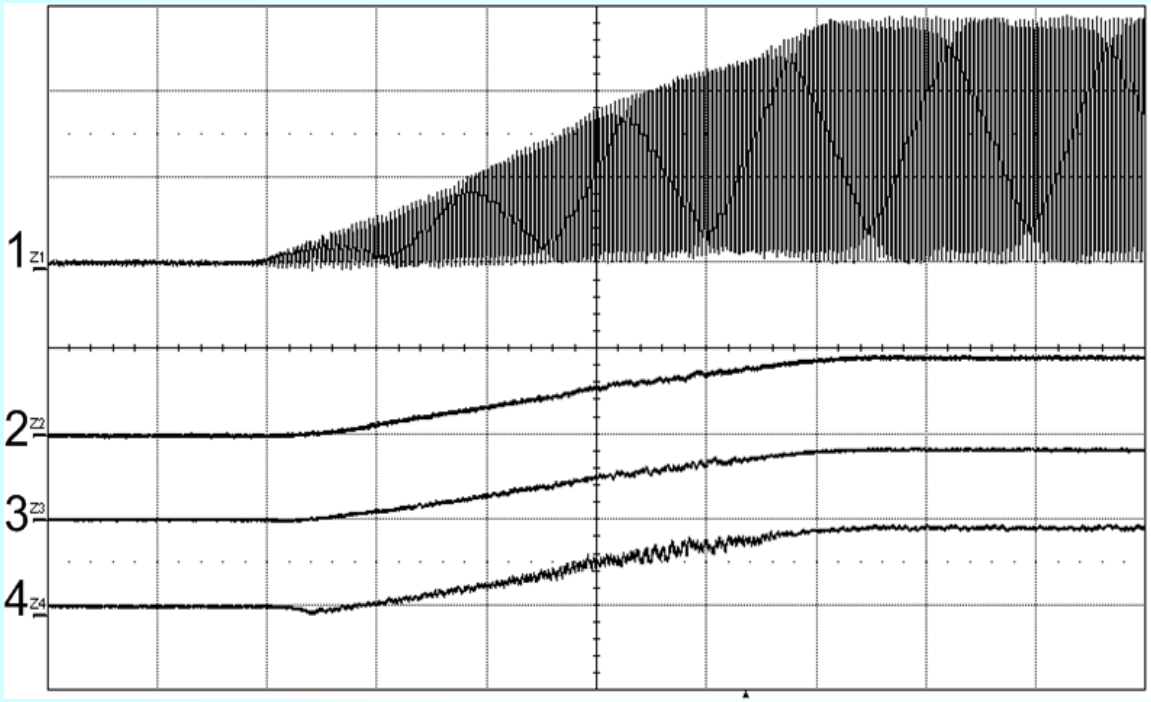
Transient performance – sudden acceleration from 6.5Hz to 40 Hz



[X-axis: 5ms/div]

1. Pole voltage [Y-axis: 70V/div]
2. Capacitor-CA1 voltage ripple. [100V/div]
3. Capacitor-CA2 voltage ripple. [50V/div]
4. Capacitor-CA3 voltage ripple. [25V/div]

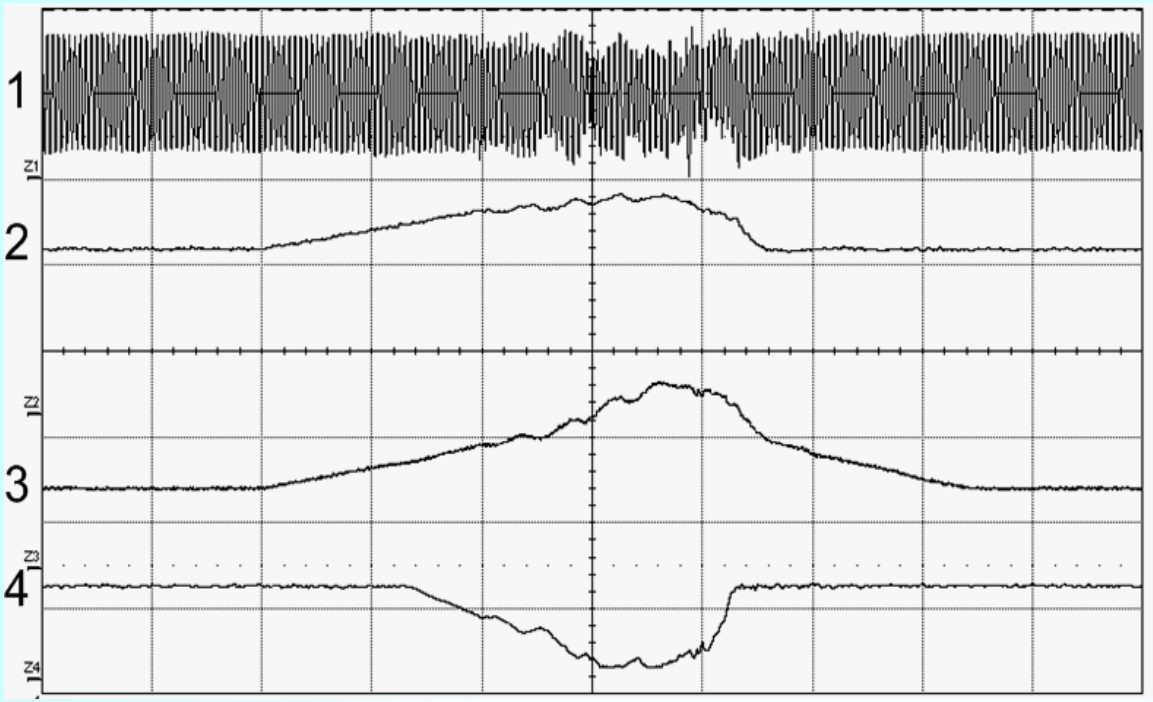
Automatic charging of the capacitors when the inverter is switched ON



[X-axis: 5ms/div]

1. Pole voltage [Y-axis: 60V/div]
2. Capacitor-CA1 voltage ripple. [100V/div]
3. Capacitor-CA2 voltage ripple. [50V/div]
4. Capacitor-CA3 voltage ripple. [20V/div]

Testing of capacitor voltage balancing scheme

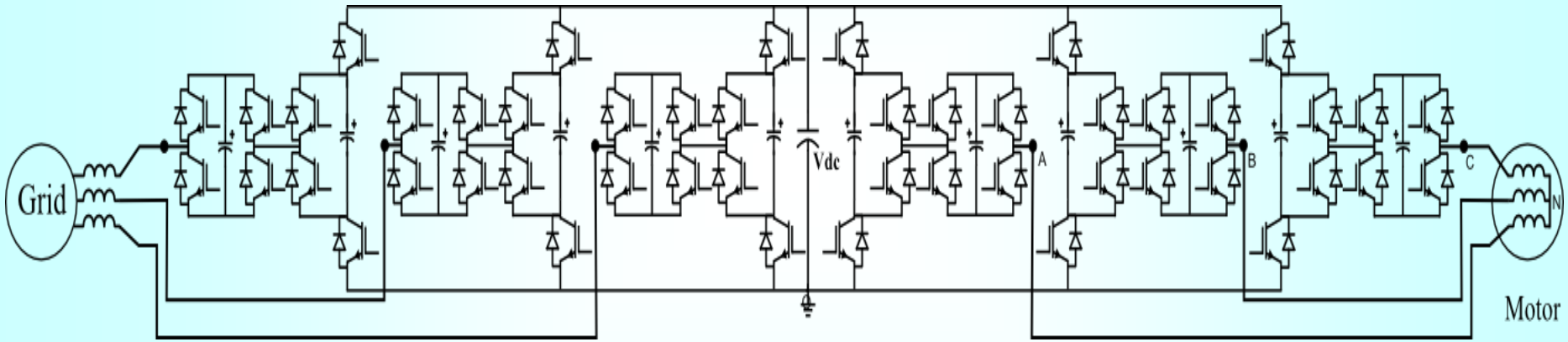


[X-axis: 500ms/div]

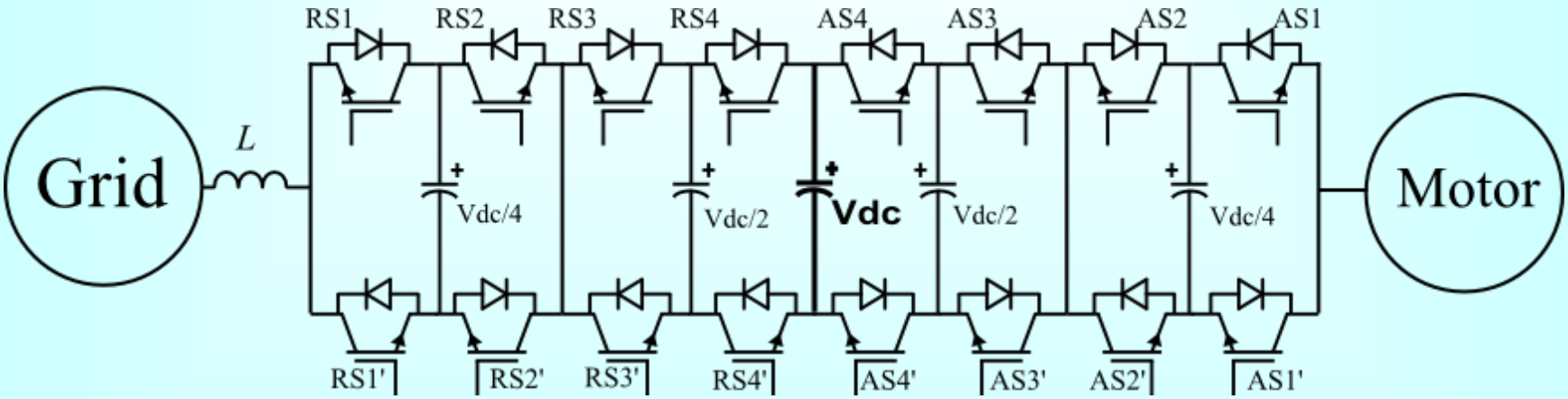
1. Pole voltage [Y-axis: 60V/div]
2. Capacitor-CA1 voltage ripple. [50V/div]
3. Capacitor-CA2 voltage ripple. [30V/div]
4. Capacitor-CA3 voltage ripple. [25V/div]

Pole Voltage and Capacitor voltage wave forms in A-phase when the capacitor voltage balancing scheme is momentarily disabled

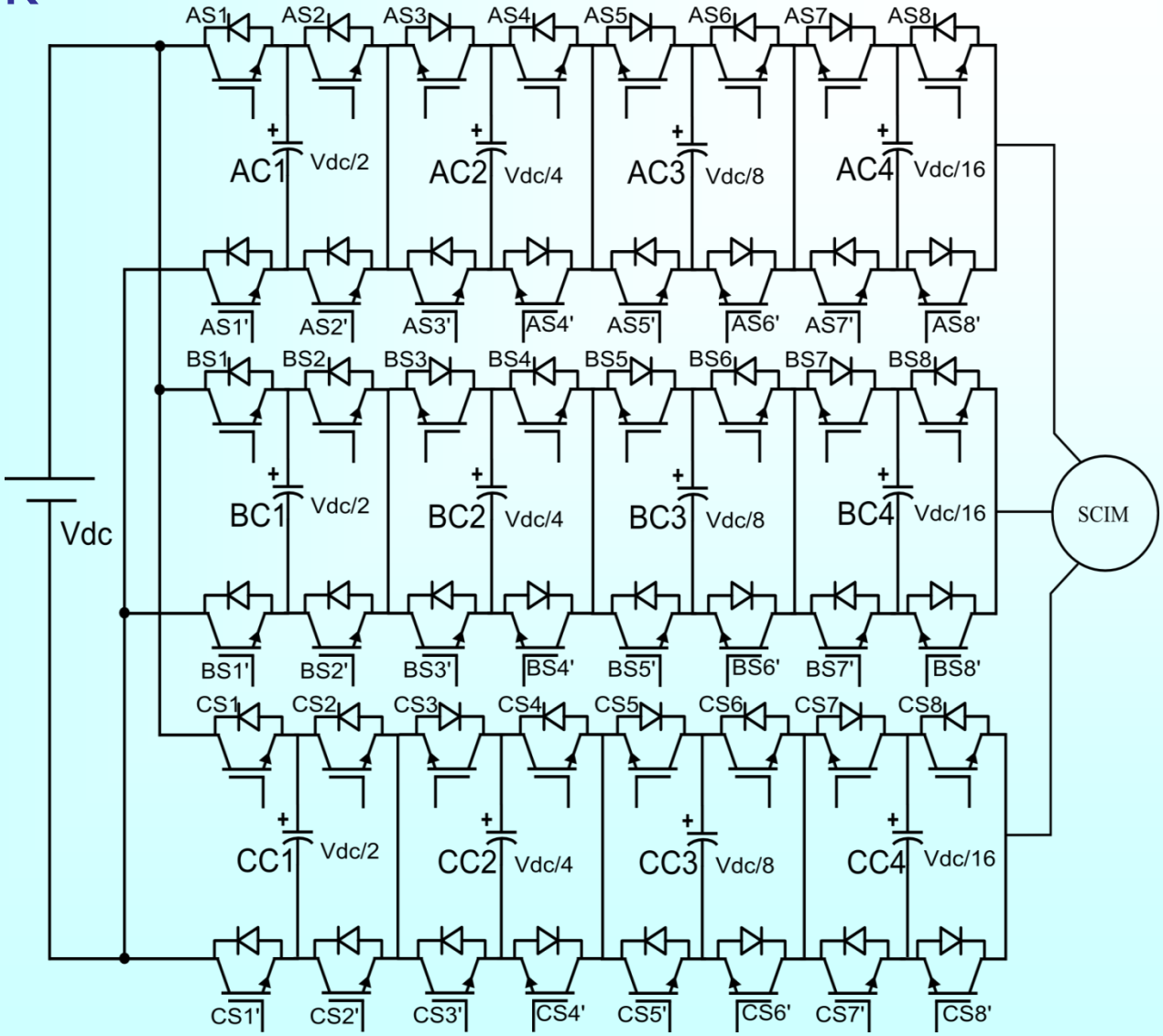
Five level Back to Back converter



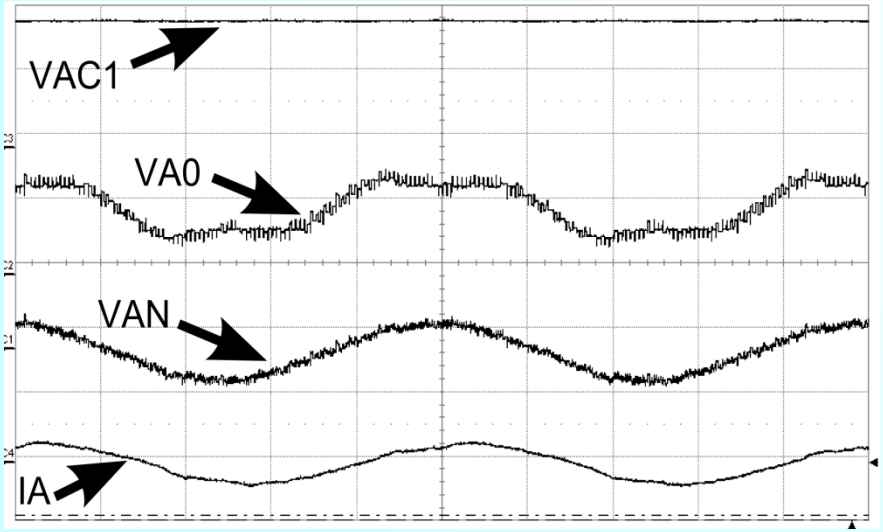
Fivelevel Back to Back converter - Single leg



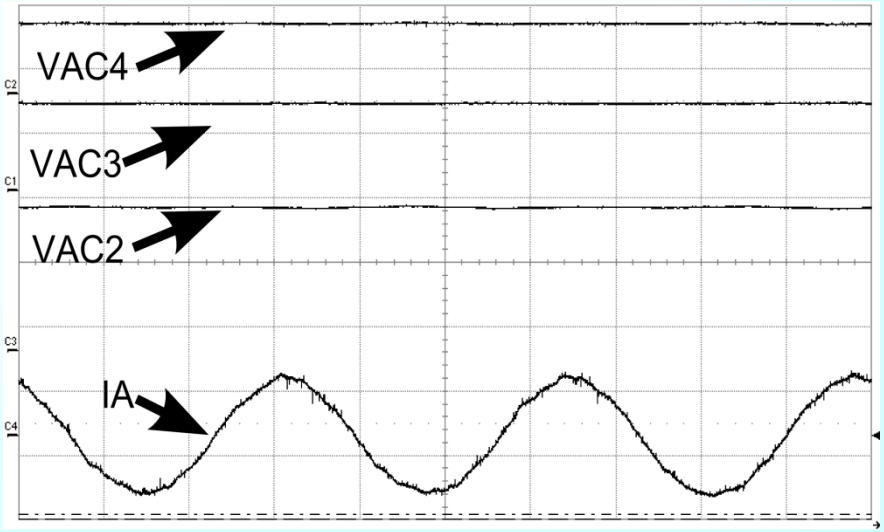
3-Phase 17-level Power Circuit With Single DC link



20Hz operation

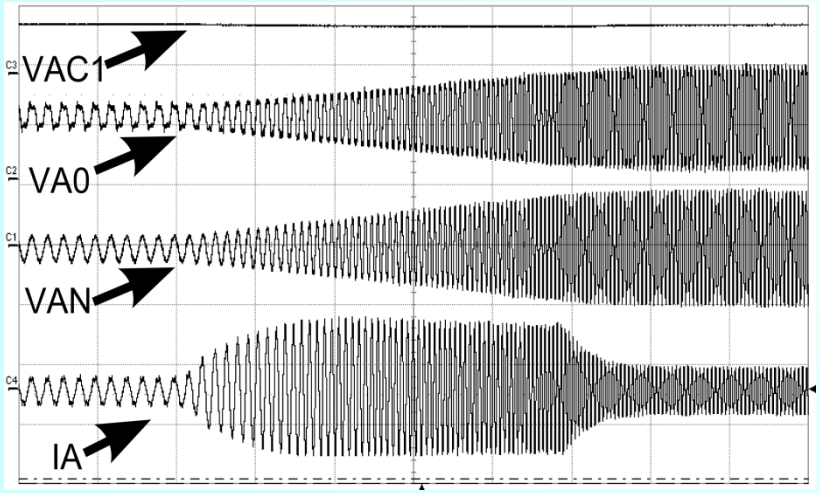


VAC1: (50V/div), VAO: Pole voltage(100V/div), VAN: Phase Voltage (100V/div), IA: 2A/div, Timescale: (10mS/div).

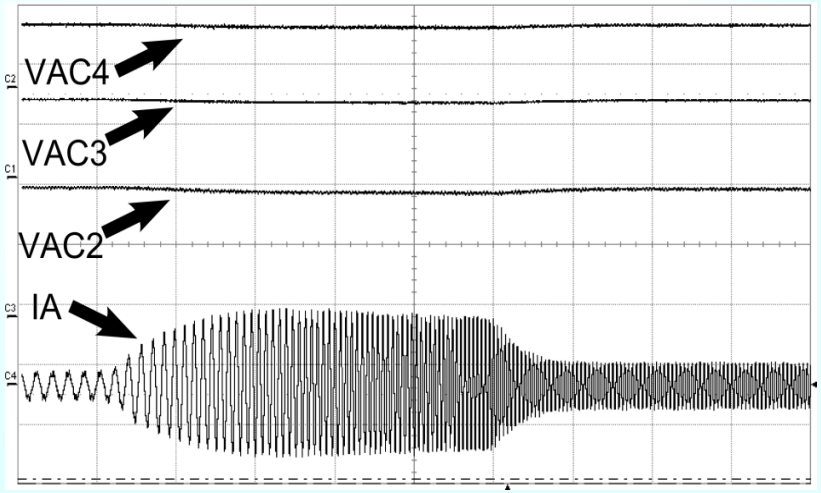


VAC4: (20V/div), VAC3: (10V/div), VAC2: (25V/div), IA:2A/div, Timescale: 10mS/div

Acceleration Profile

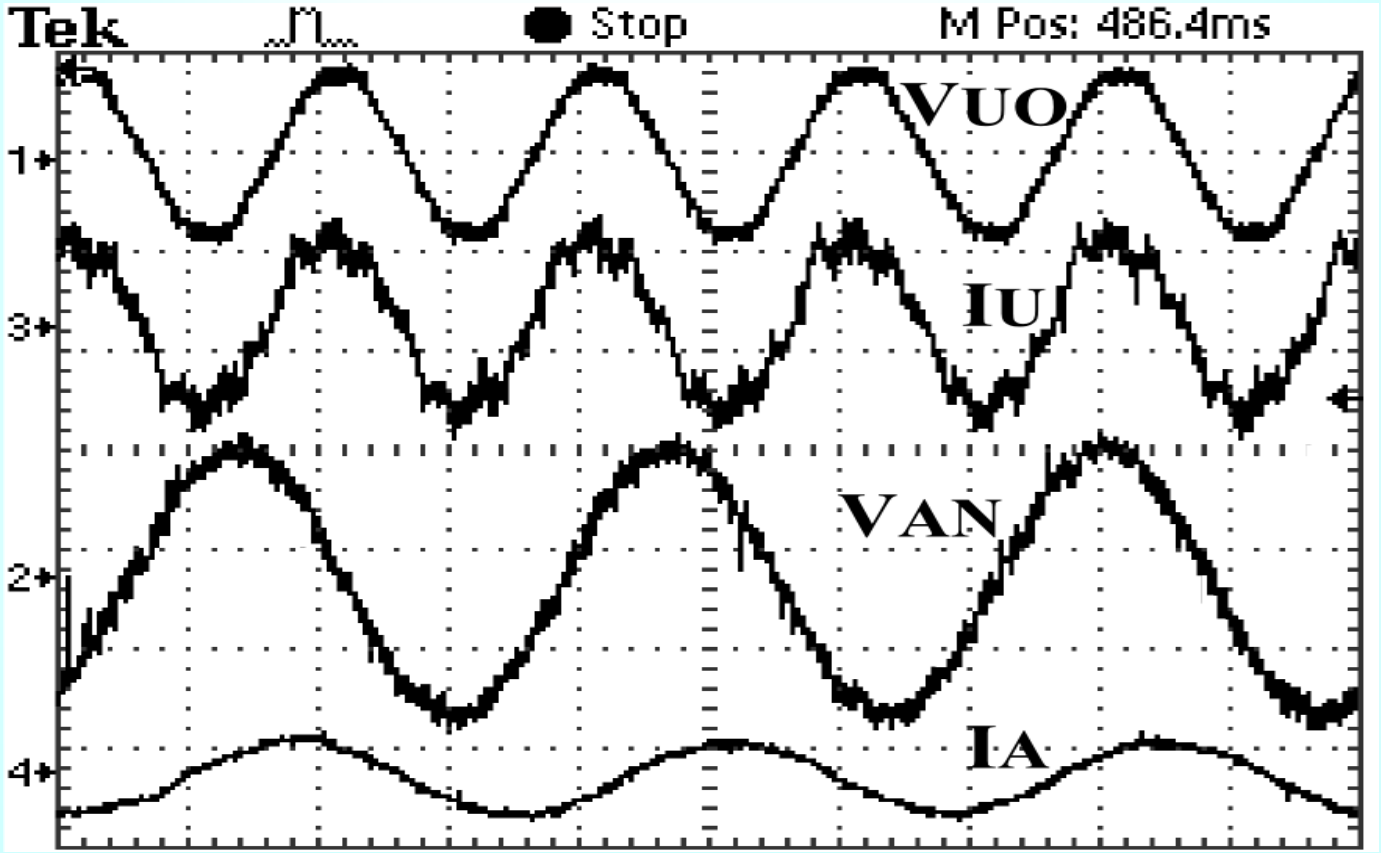


VAC1:Cap AC1 voltage(100V/div),
VAO: Pole Voltage(100V/div) ,
VAN: Phase Voltage(100V/div),
IA: Phase current(2A/div)
Timescale (500mS/div)

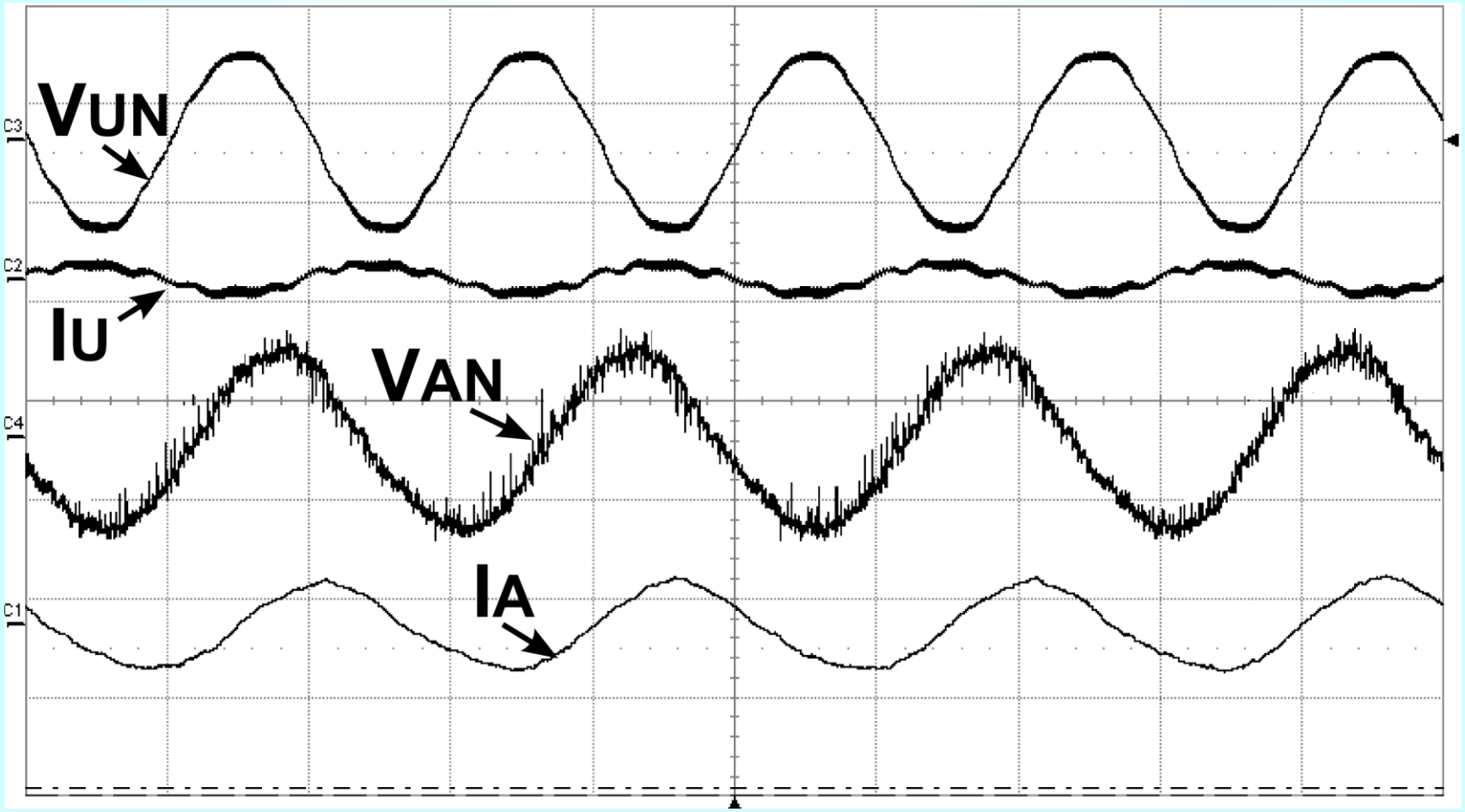


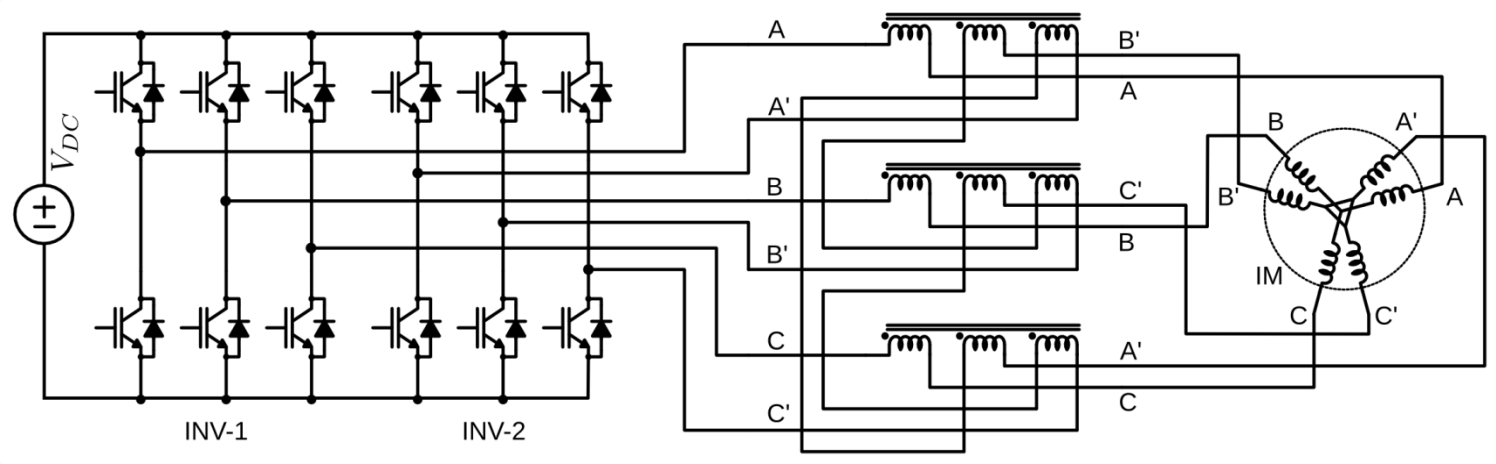
VAC4:Cap AC4 voltage(10V/div),
VAC3:Cap AC3 voltage (20V/div),
VAC2:Cap AC2 voltage (20V/div),
IA: Phase current(2A/div)
Timescale (500mS/div)

Motoring Mode- with nearly unity power factor and sinusoidal current from the Mains

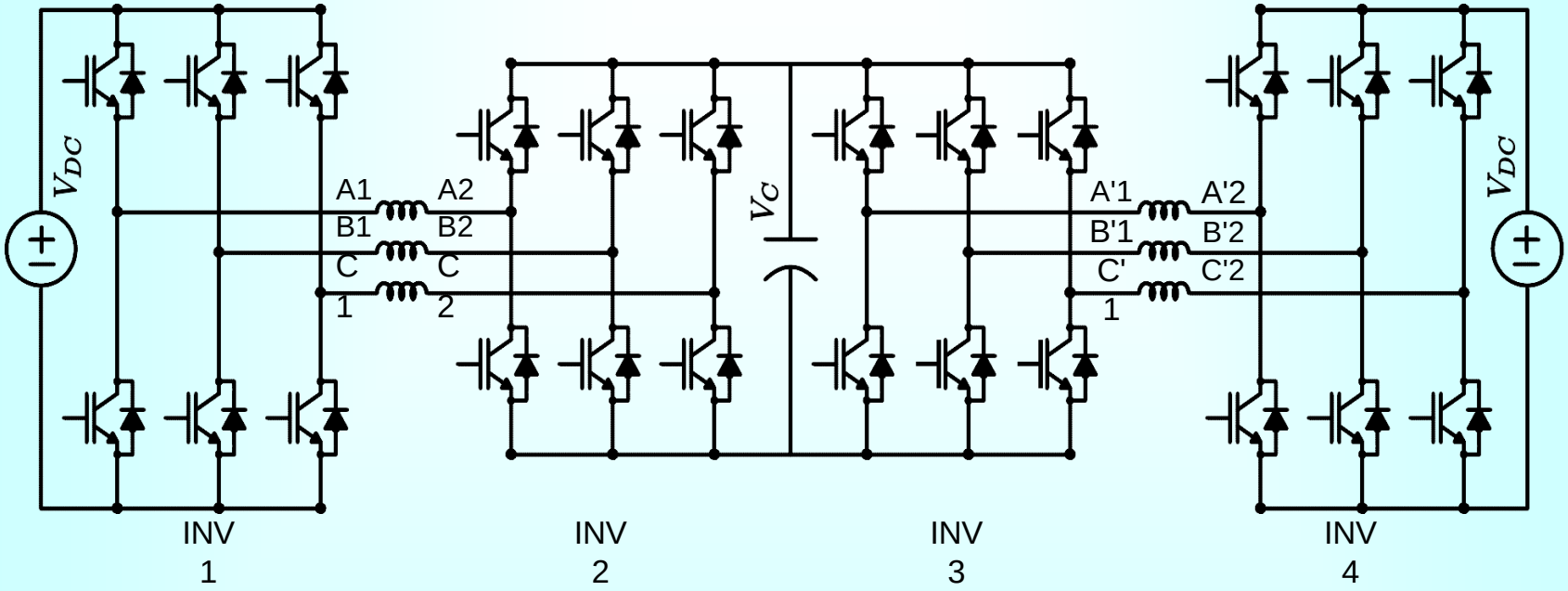


Regeneration




V_{DC}
INV-1
INV-2
A
A'
B
B'
C
C'
B'
A
C'
B
A'
C
IM
B
A'
B'
A
C
C'

Proposed Power Circuit

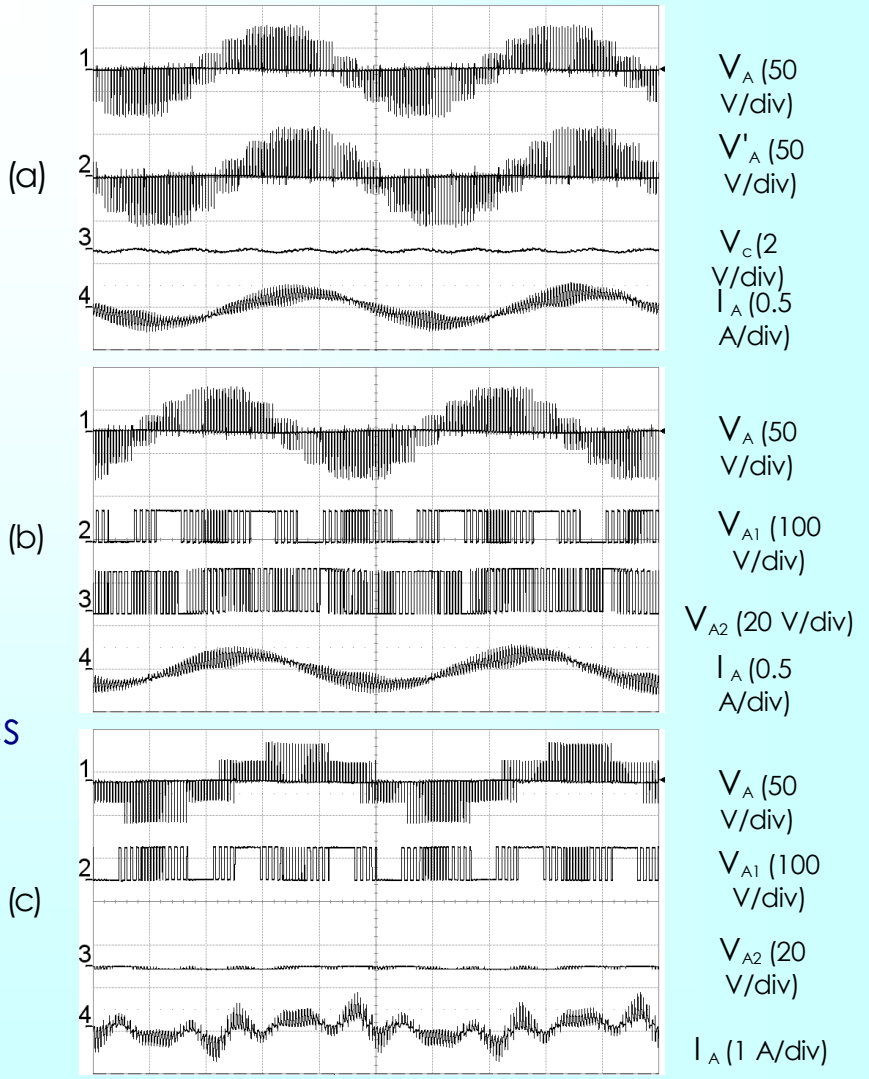


- Replace DC-link V_{dc} with capacitor of voltage V_c
- Average the two possible (45' and 36') vectors to take zero net power from the capacitor

Experimental Results

Steady State waveforms @10 Hz

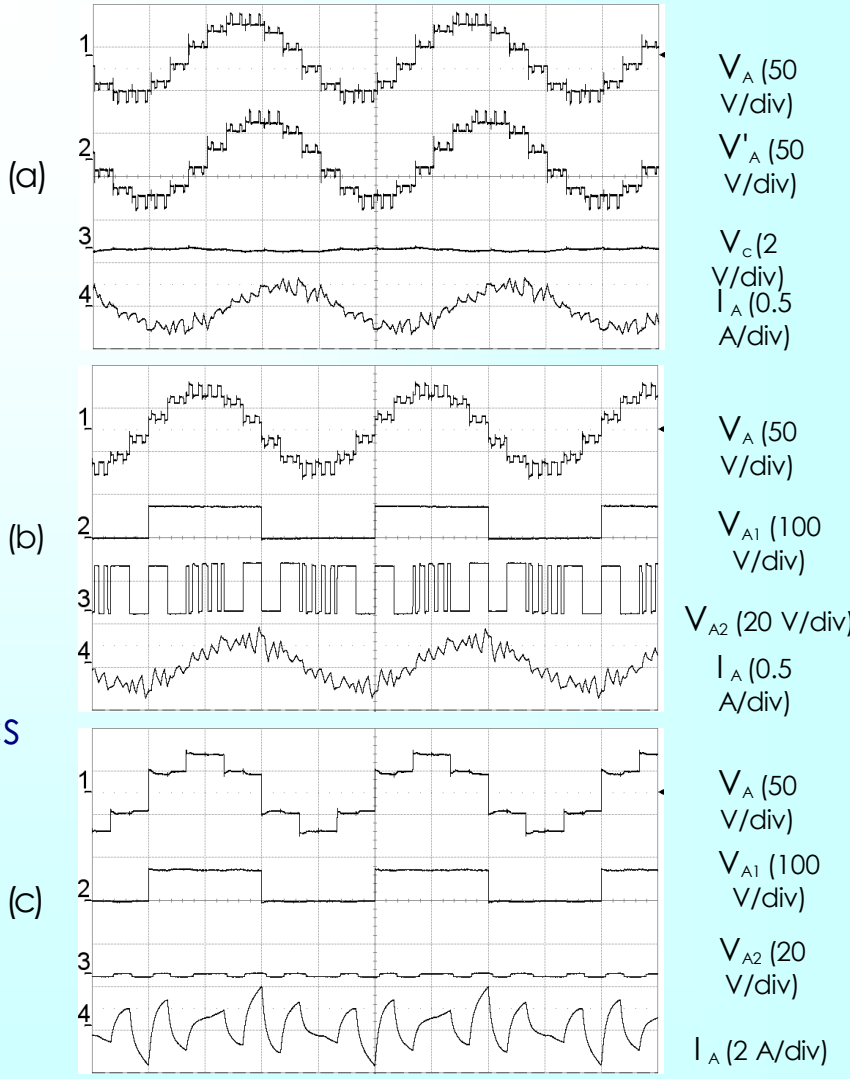
- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering Secondary inverters not switched
  - Current - high 5th and 7th order harmonics



Experimental Results

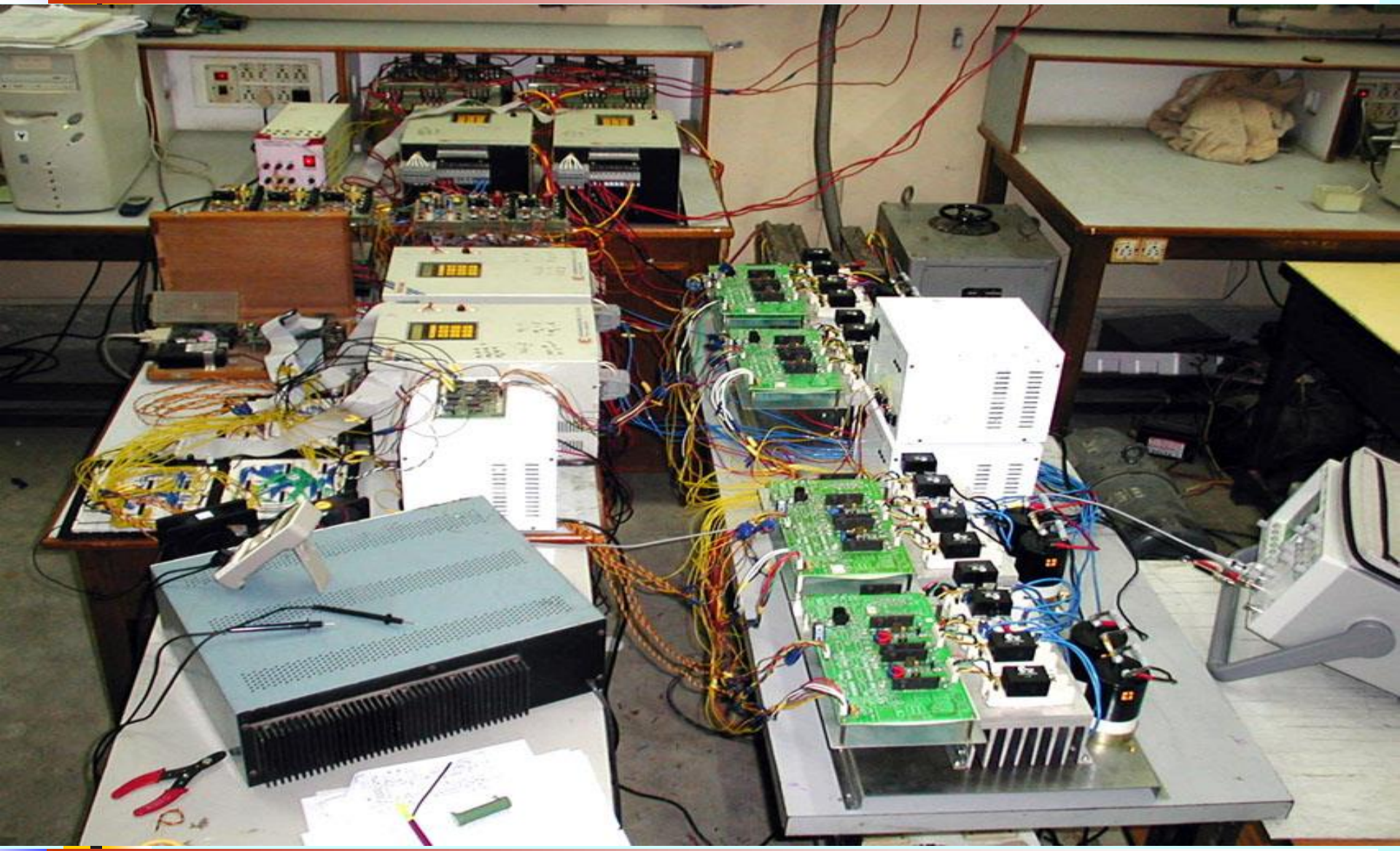
Steady State waveforms @50 Hz

- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering Secondary inverters not switched
  - Current - high 5th and 7th order harmonics



Inverter setup for multilevel structure

Inverter setup for multilevel structure



Thank you