DEVELOPMENT OF MULTI LEVEL INVERTER TOPOLOGIES

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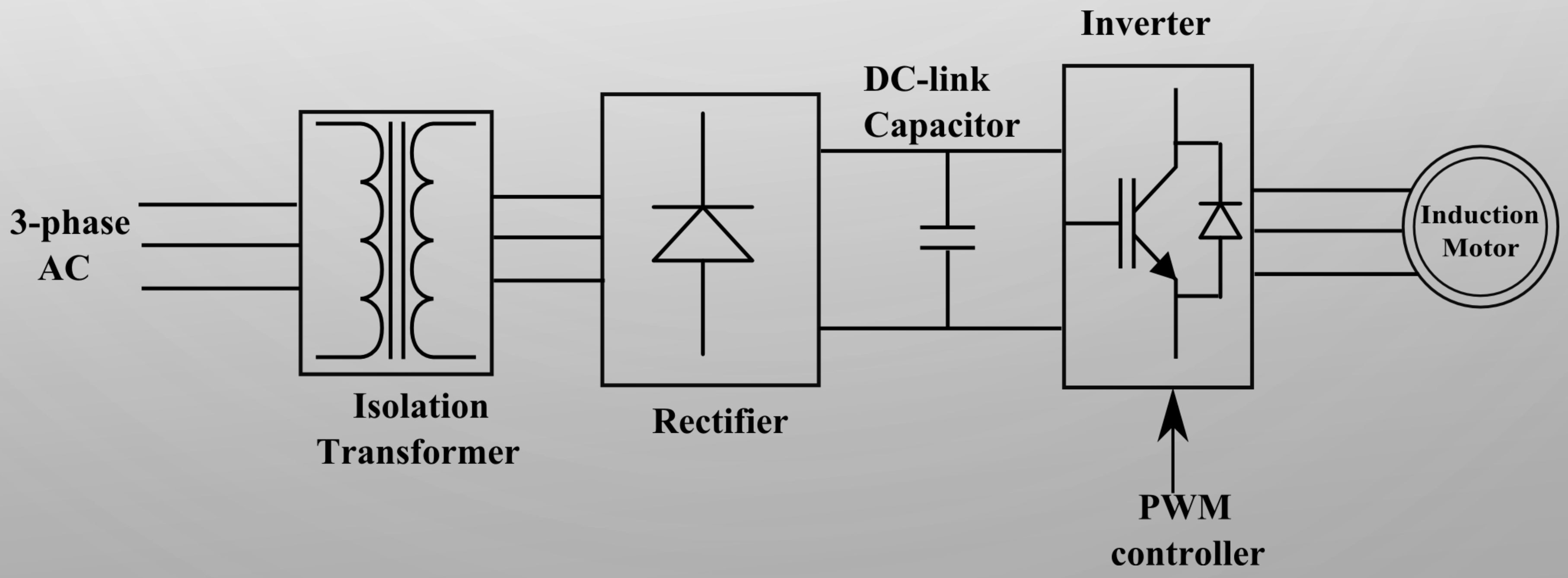
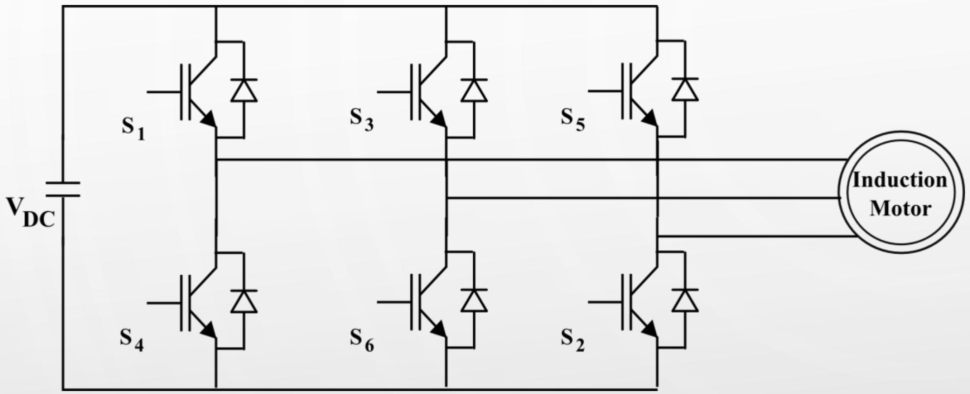
Introduction

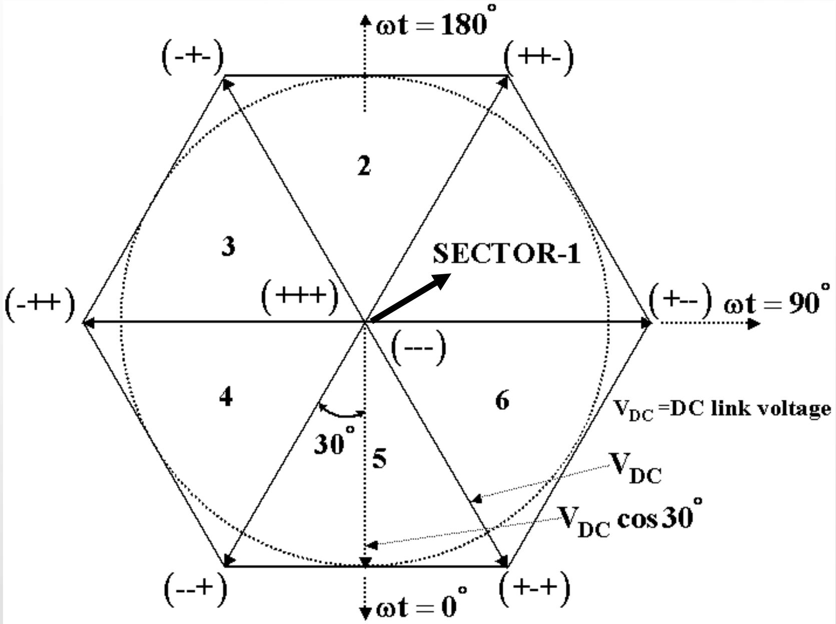
A VSI fed conventional IM drive



Two-level Inverter



Two-level Voltage Source Inverter



Voltage space phasor vector locations

Where, the space vector V_r constituted by the pole voltages $v_{AO,}$ v_{BO} and v_{CO} is defined as:

$$V_r = v_{AO} + v_{BO}e^{j120^o} + v_{CO}e^{j120^o}$$

$$T_0 = T_s - (T_1 + T_2)$$

$$T_1 = T_s \frac{V_s}{V_{DC}} \frac{\sin(60-\alpha)}{\sin 60} \qquad T_2 = T_s \frac{V_s}{V_{DC}} \frac{\sin\alpha}{\sin 60}$$

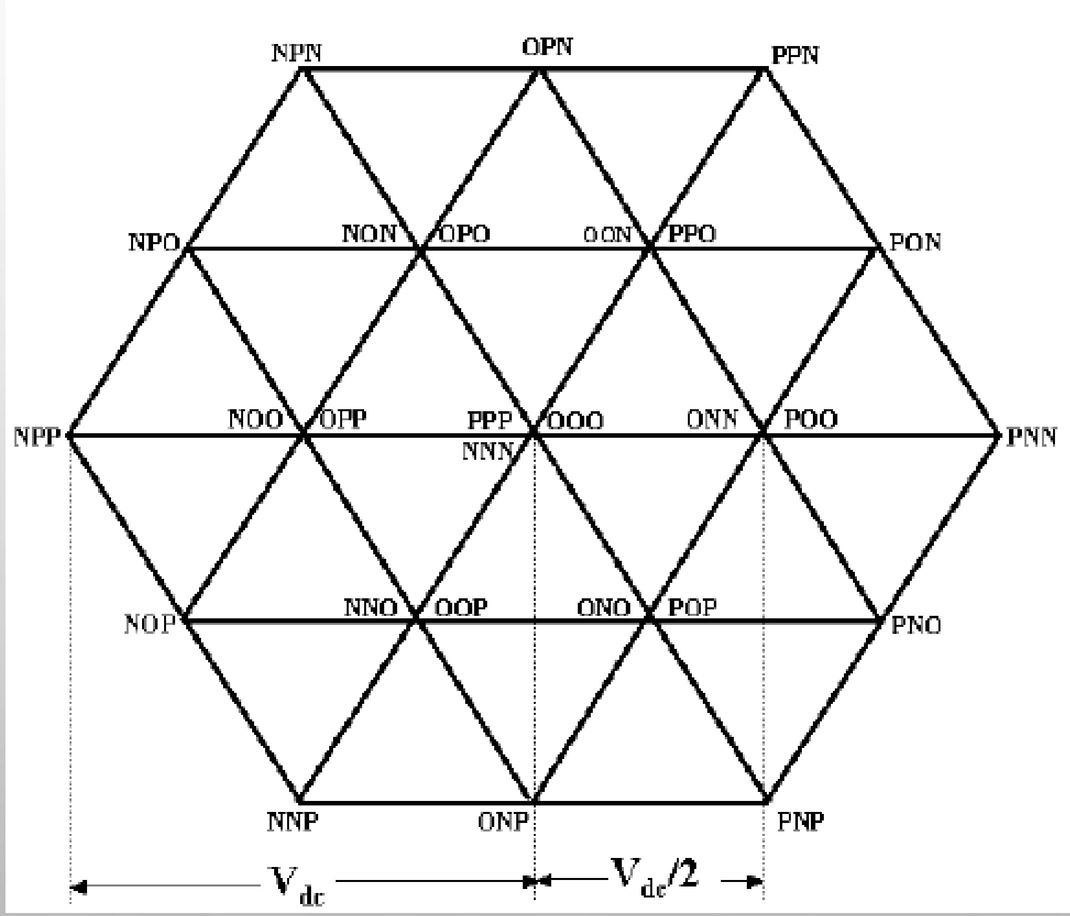
Vector

If each leg of inverter is capable to produce three voltage levels

Leg 1	Leg 2	Leg 3
+	+	+
+	+	0
+	0	0
-	-	-

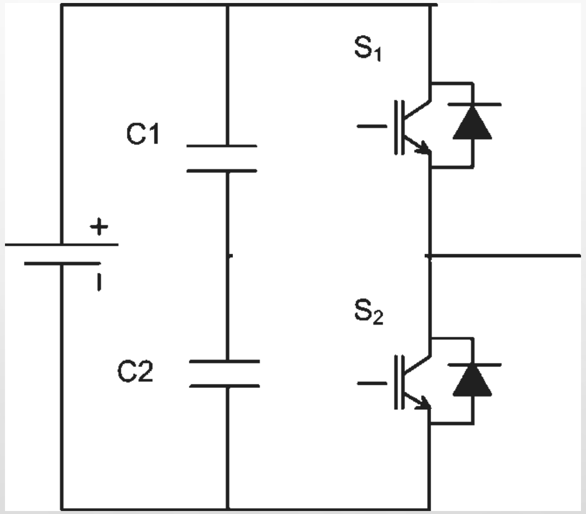
Total of 27 (3^3)combinations are possible

How will be the space vector diagram with these 27 switching combinations

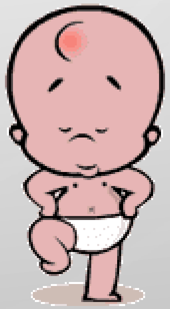


How to realize ?

Possible Power circuit for Three-level inverter



But what kind of switch is suitable ?



If C1=C2

Possible output voltage levels are Vdc/2, 0 and -Vdc/2

Selection of Switch

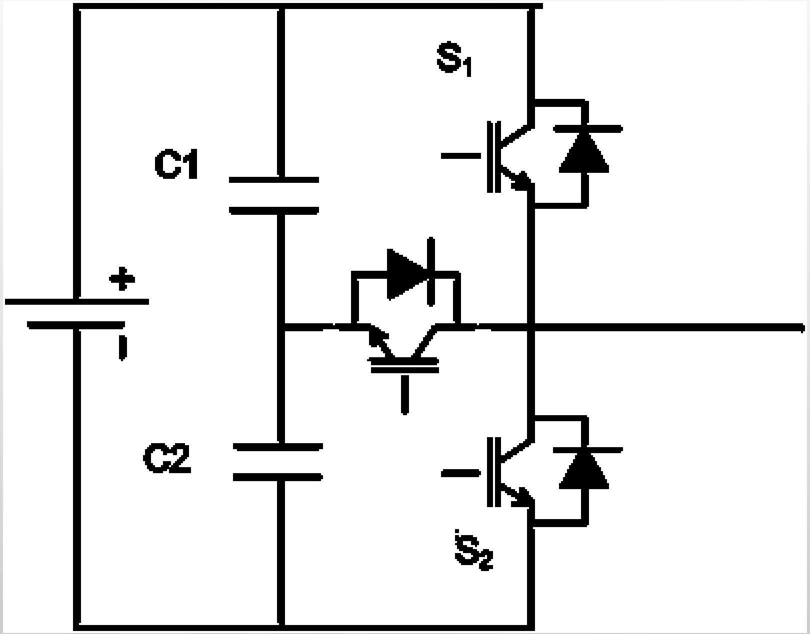
As a beginner

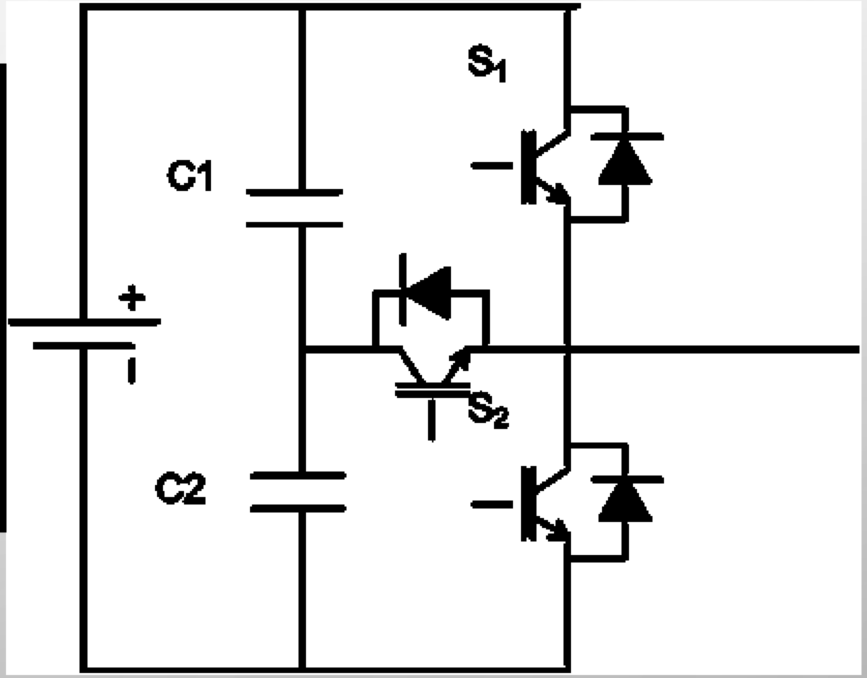
IGBT with anti-parallel diode

MOSFET

directi larity

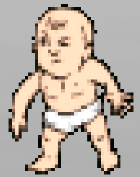
Possible Combinations:



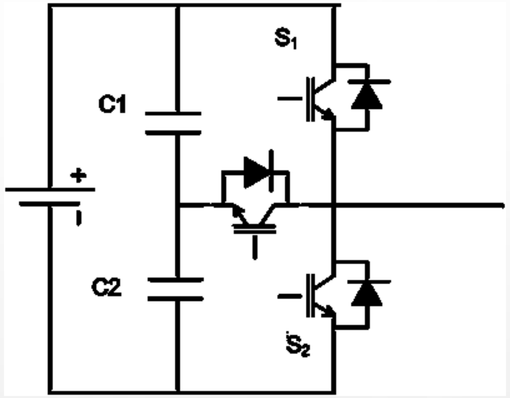


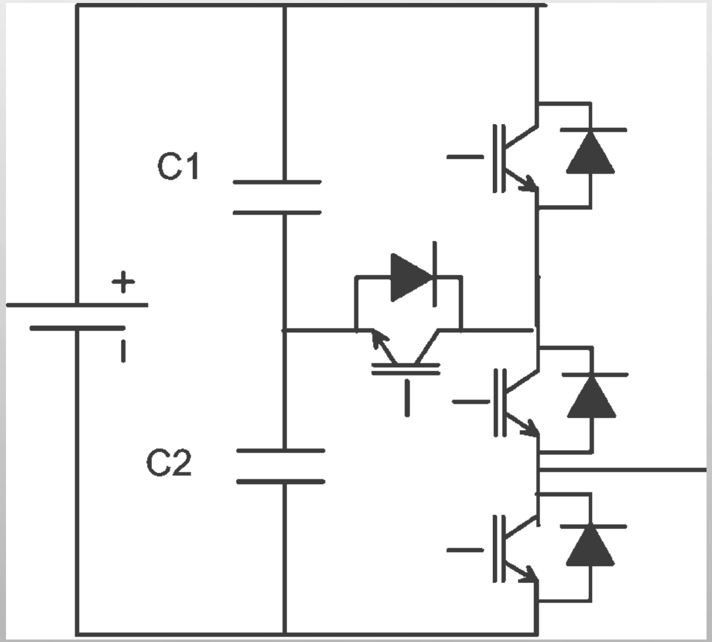
-Vdc/2 state will short ckt the Capacitor C2

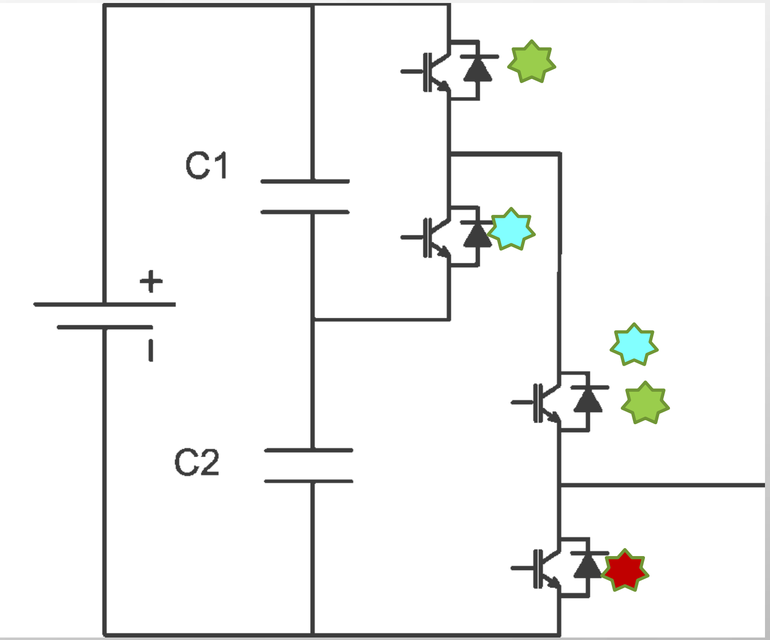
Vdc/2 state will short ckt the Capacitor C1



Cascaded Three-level Inverter

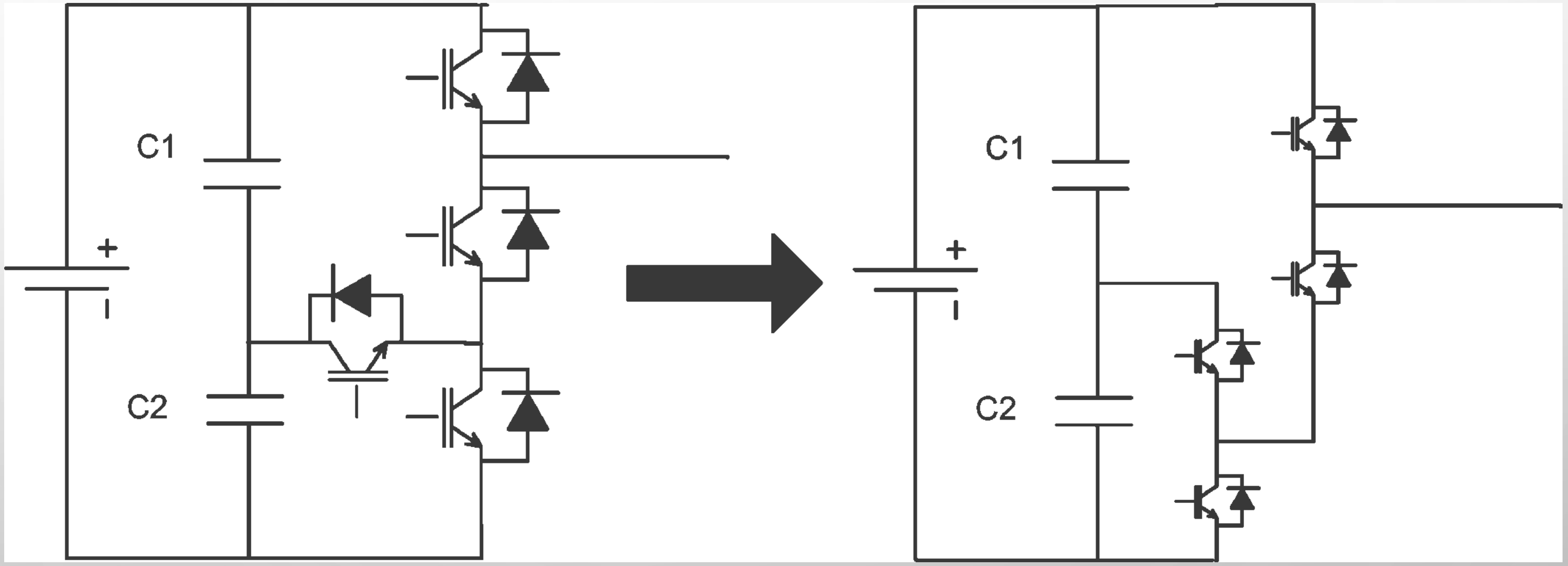






Vdc/2 0 -Vdc/2

Cascaded Three-level Inverter



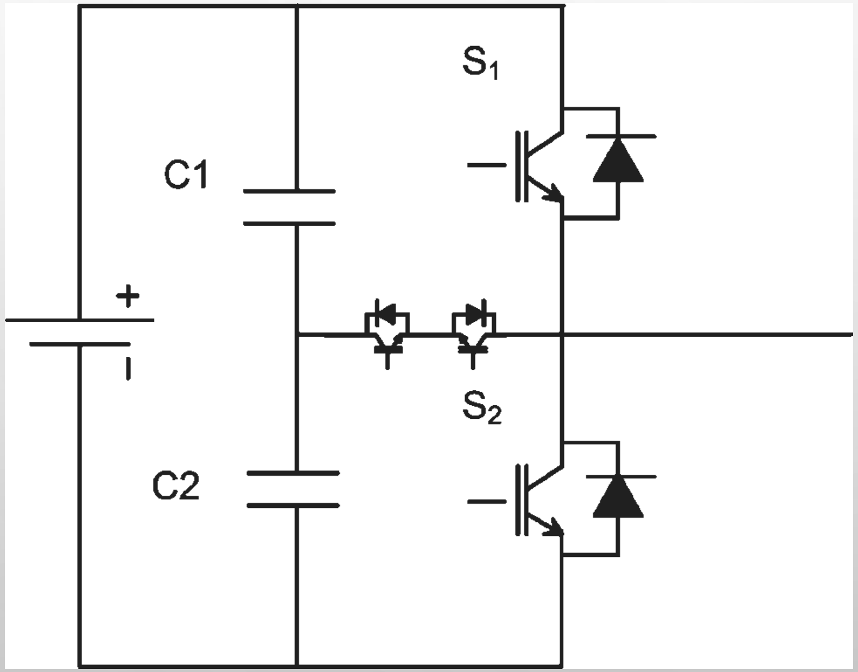
Professional Way

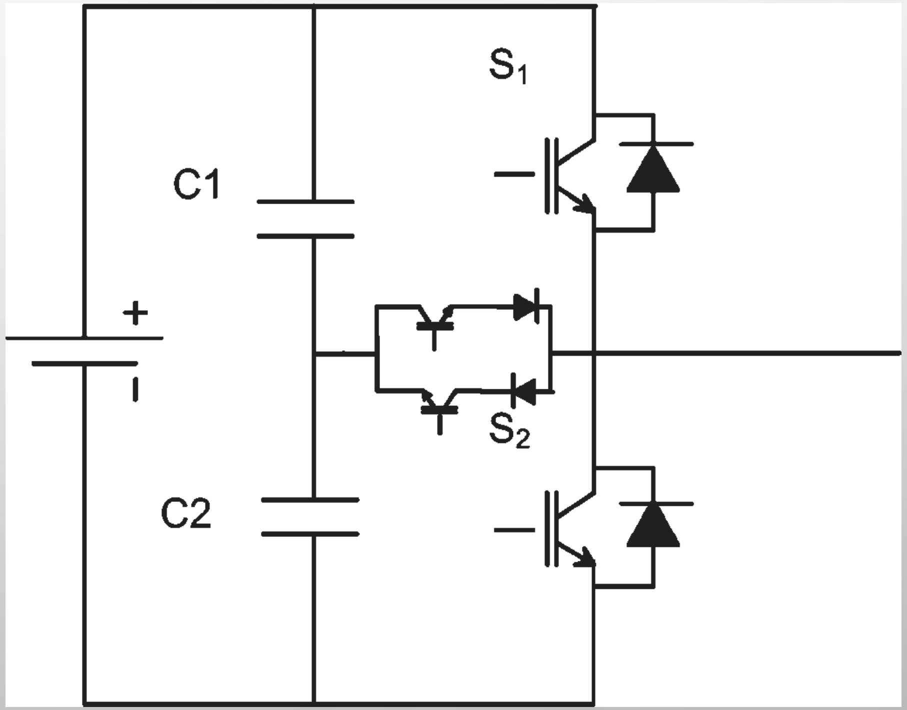
Identify the switch requirements

What kind of switch is required ?

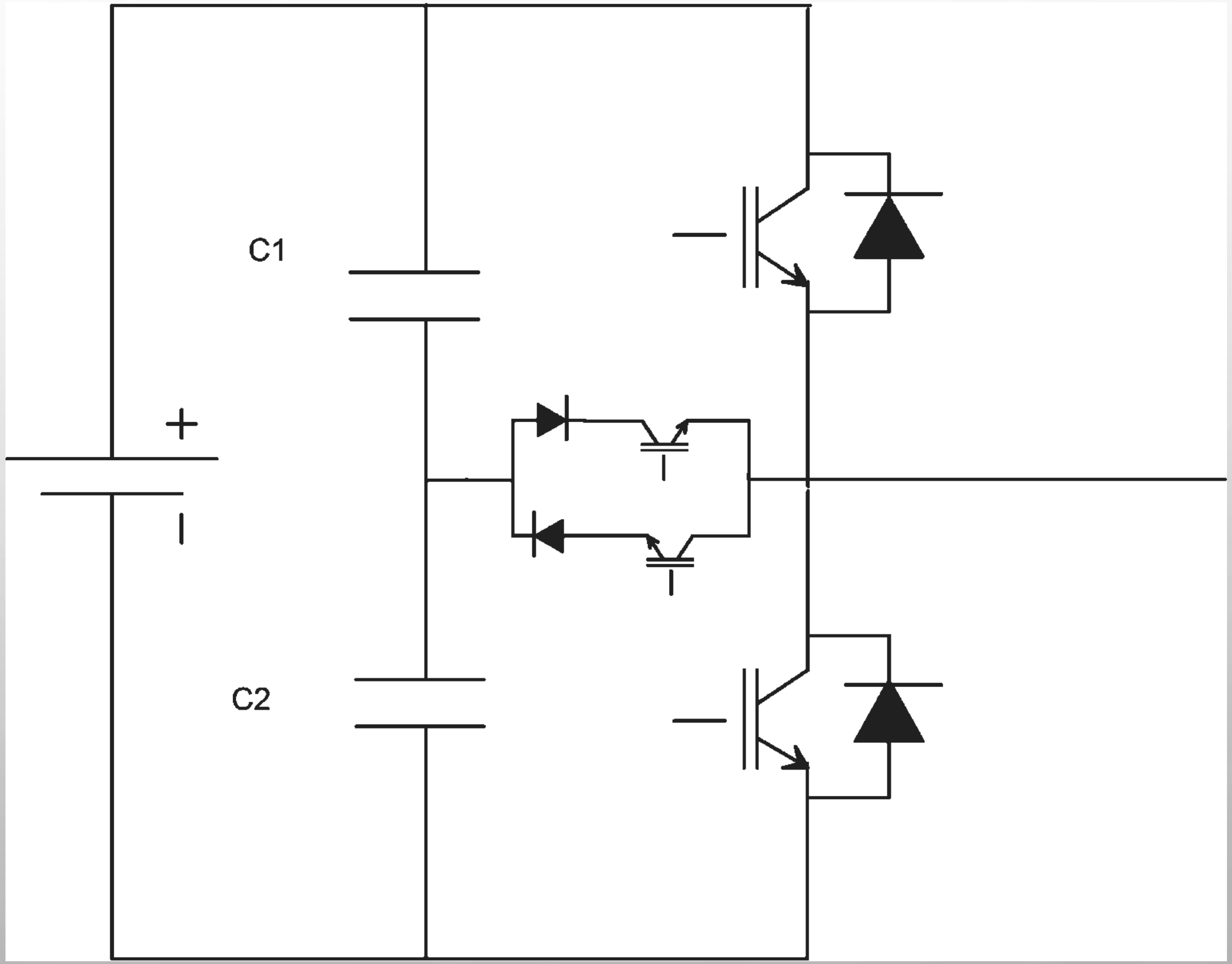
Four quadrant Switch is require

Basic Three-level Inverter

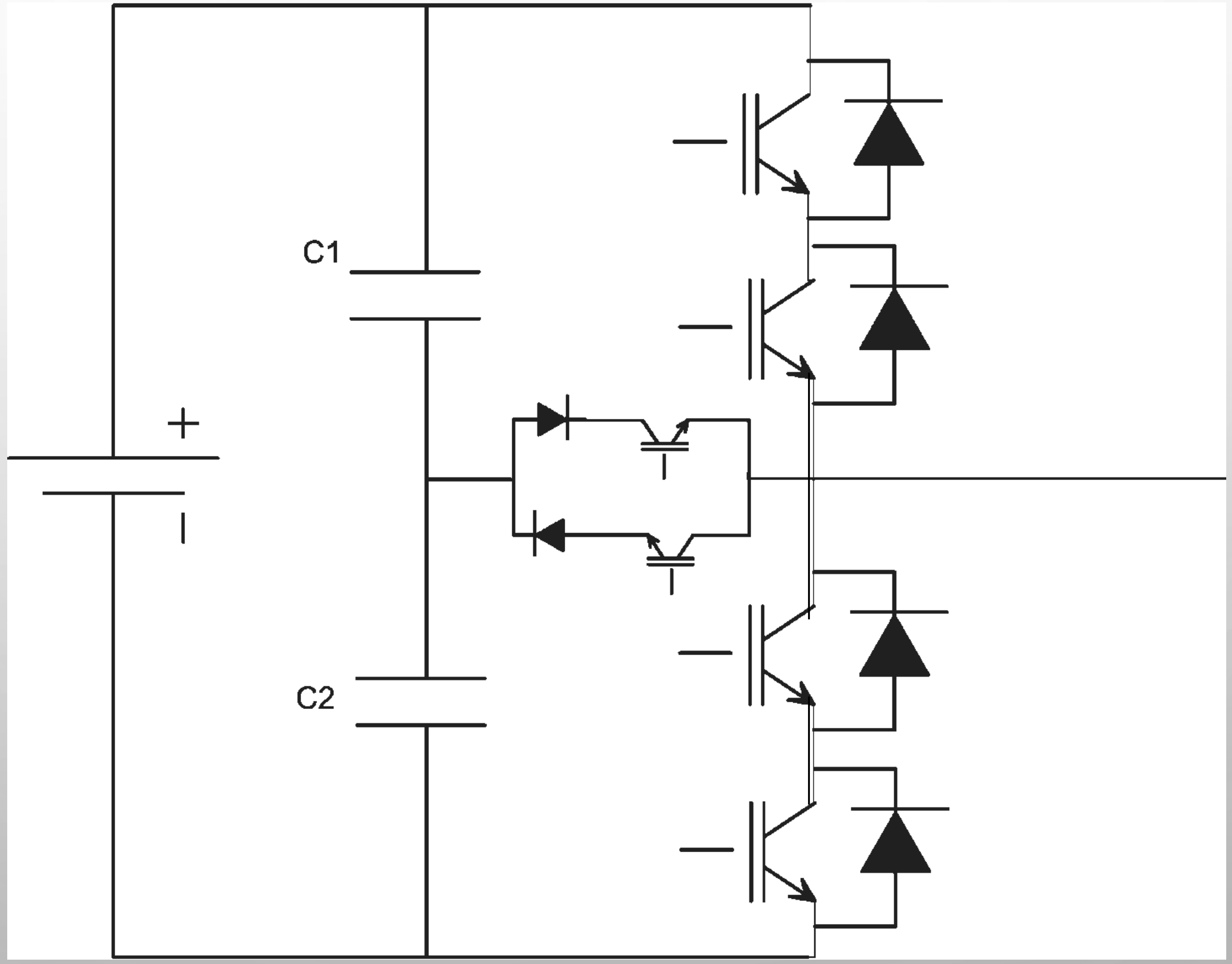




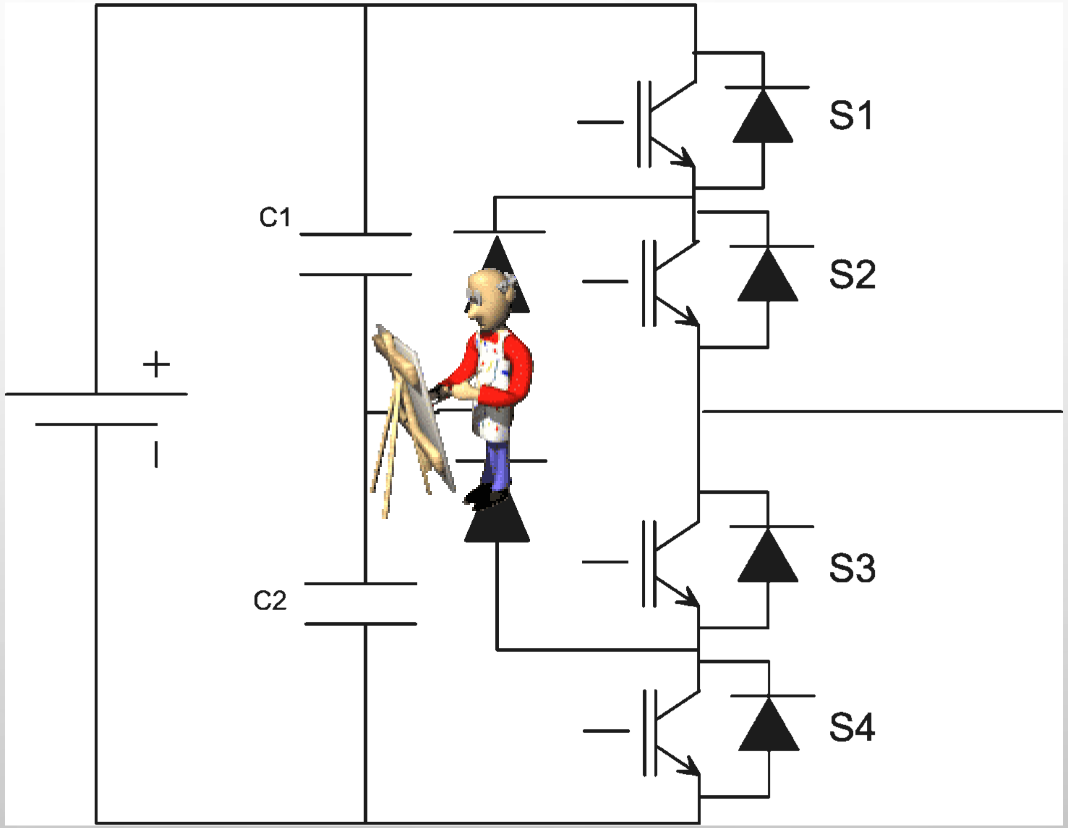
Three-Level Inverter



Three-Level Inverter



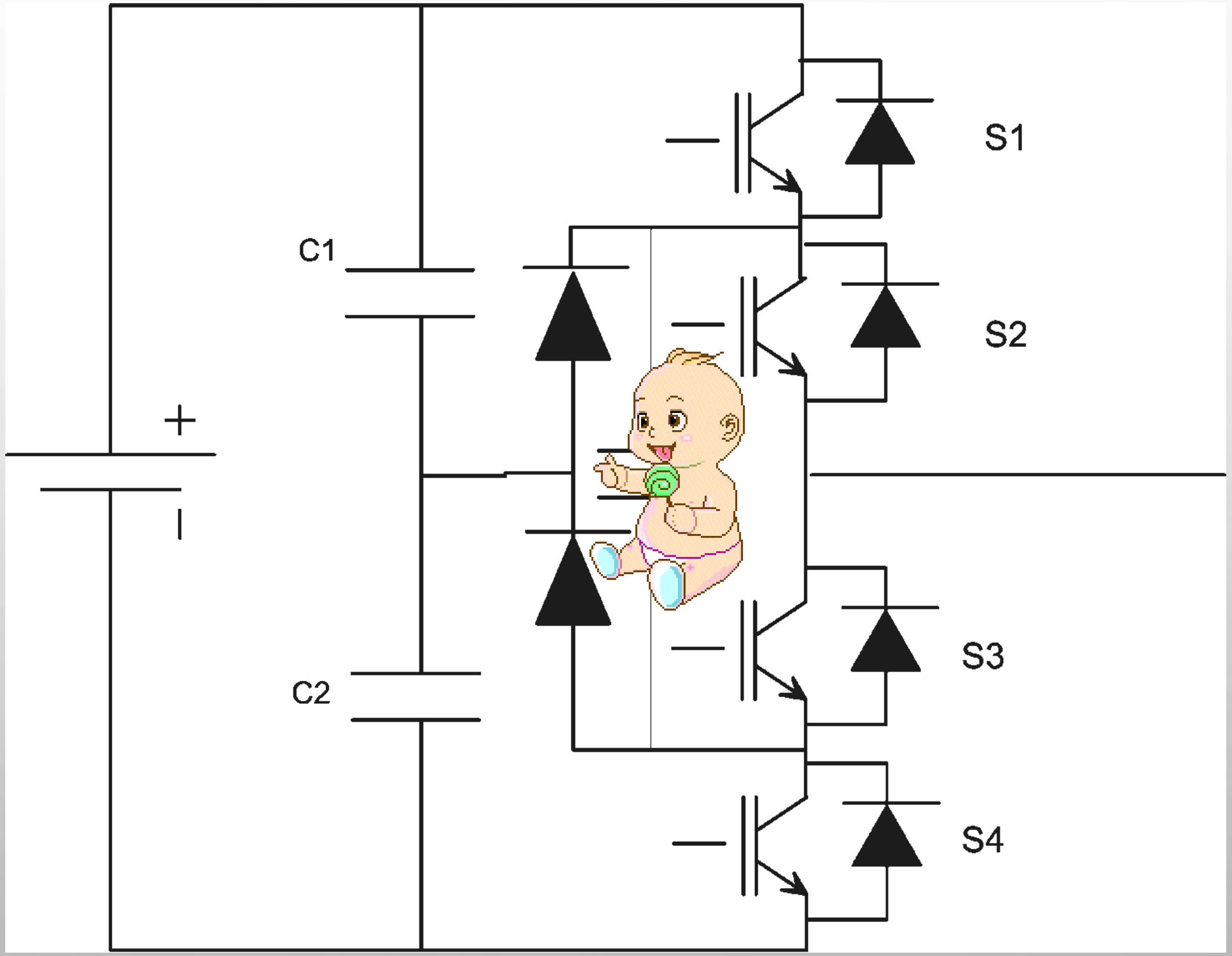
NPC Three-Level Inverter



> Capacitor Voltage balancing problem

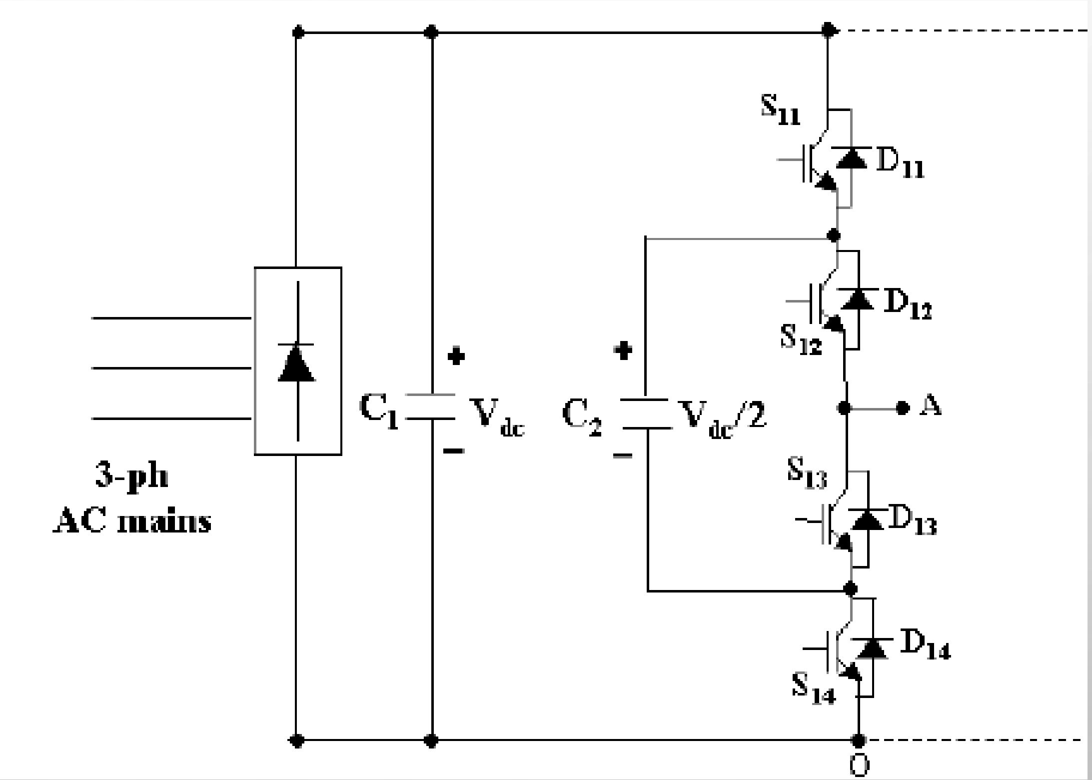
Switching condition				Output voltage
S1	S2	S3	S4	
ON	ON	OFF	OFF	Vdc/2
OFF	ON	ON	OFF	0
OFF	OFF	ON	ON	-Vdc/2

NPC Three-Level Inverter with capacitor Balancing



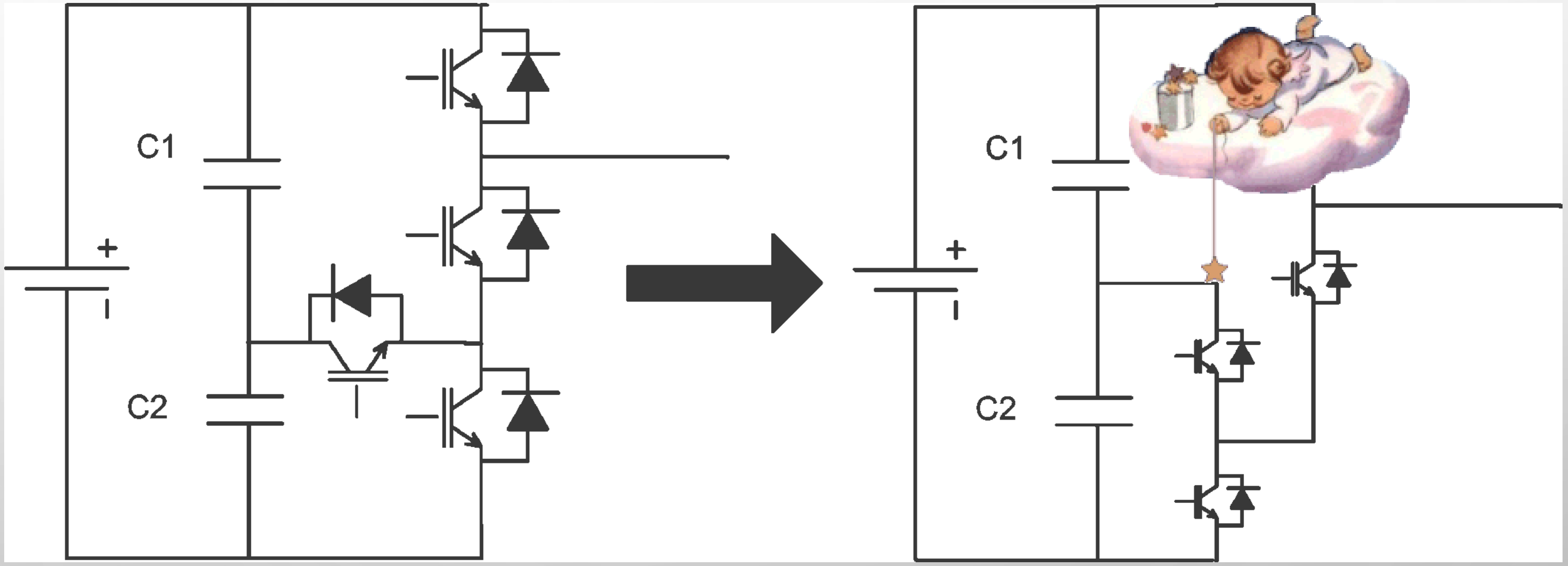
Switching condition				Output voltage
S1	S2	S3	S4	
ON	ON	OFF	OFF	Vdc/2
ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	0
OFF	OFF	ON	ON	-Vdc/2

Multilevel Inverters with Flying Capacitor Configuration

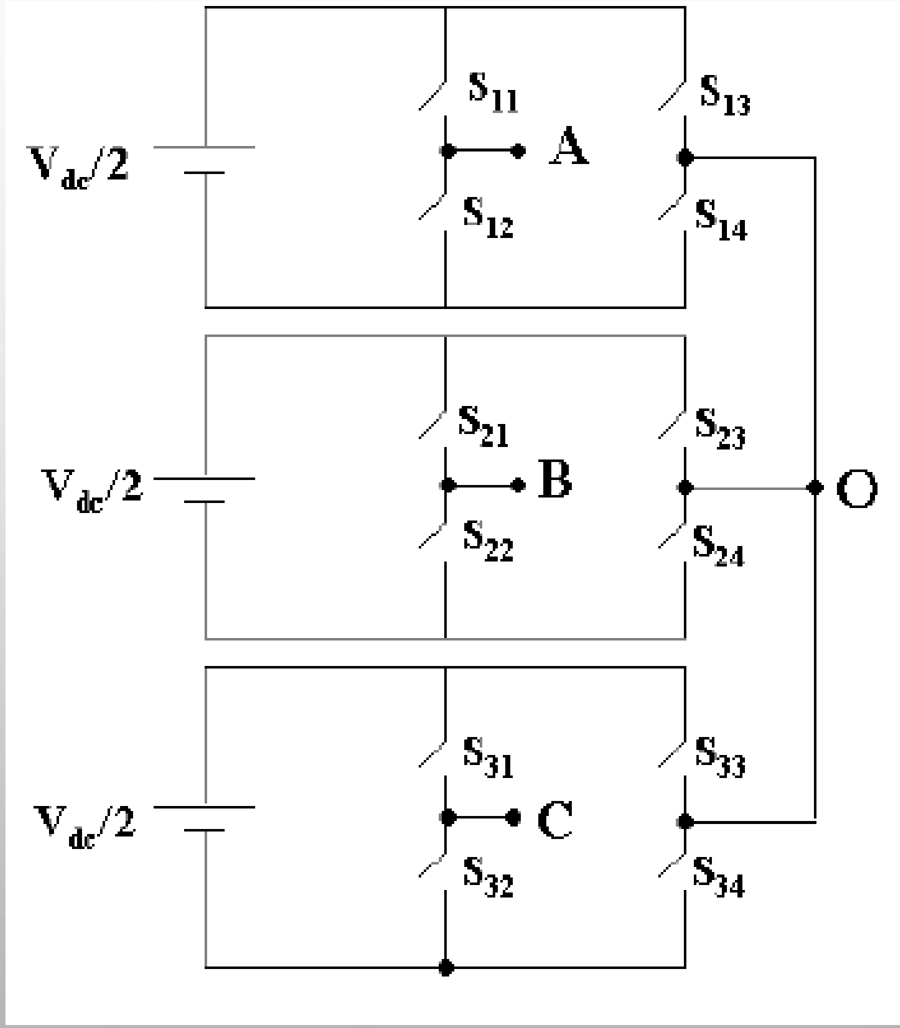


Switching conditions				Output Voltage (v_{AO})
S_{11}	S_{12}	S_{13}	S_{14}	
ON	ON	OFF	OFF	V_{dc}
ON	OFF	ON	OFF	$\frac{V_{dc}}{2}$
OFF	ON	OFF	ON	$\frac{V_{dc}}{2}$
OFF	OFF	ON	ON	0

Recollect the Cascaded Three-level Inverter

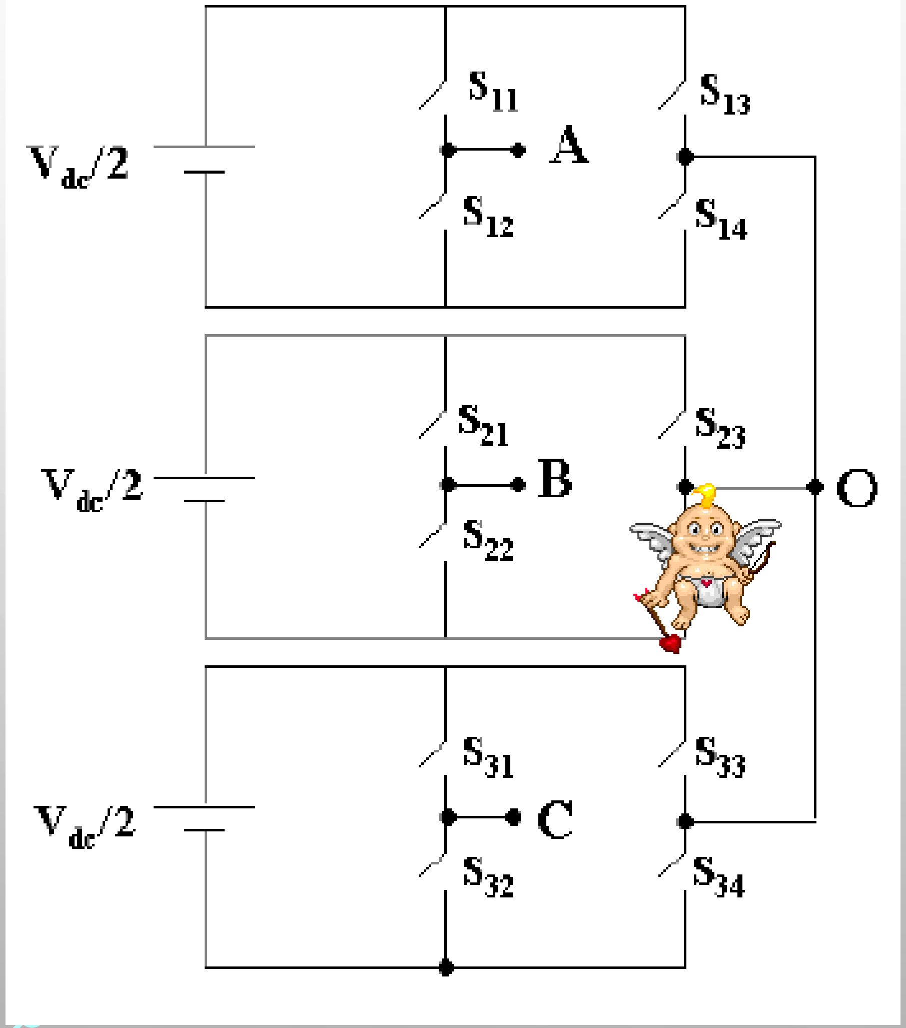


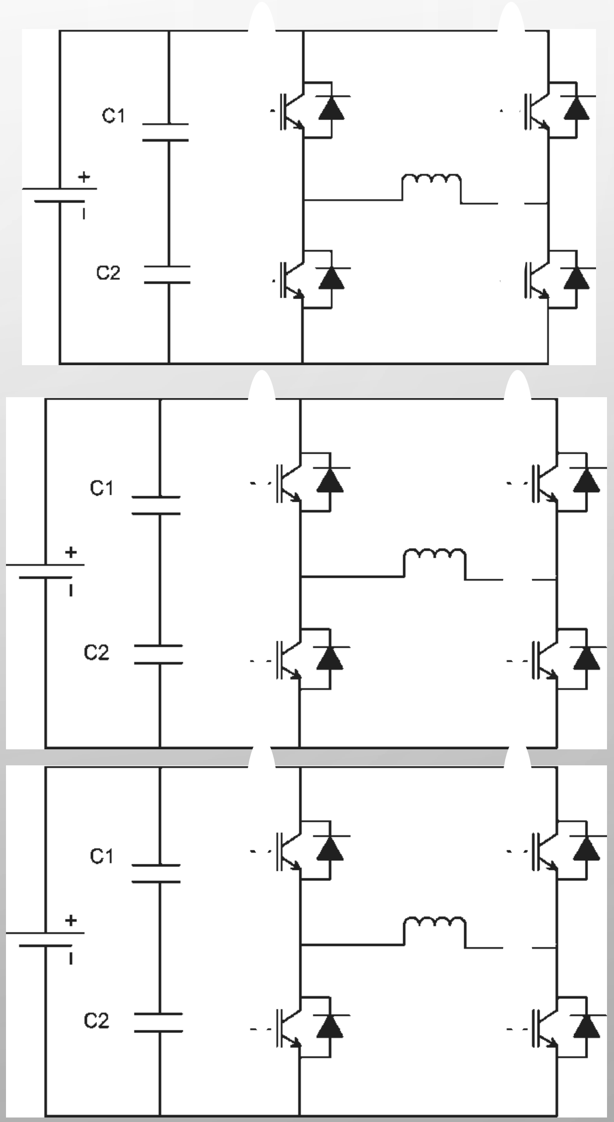
Cascaded H- bridge Three-level Inverter



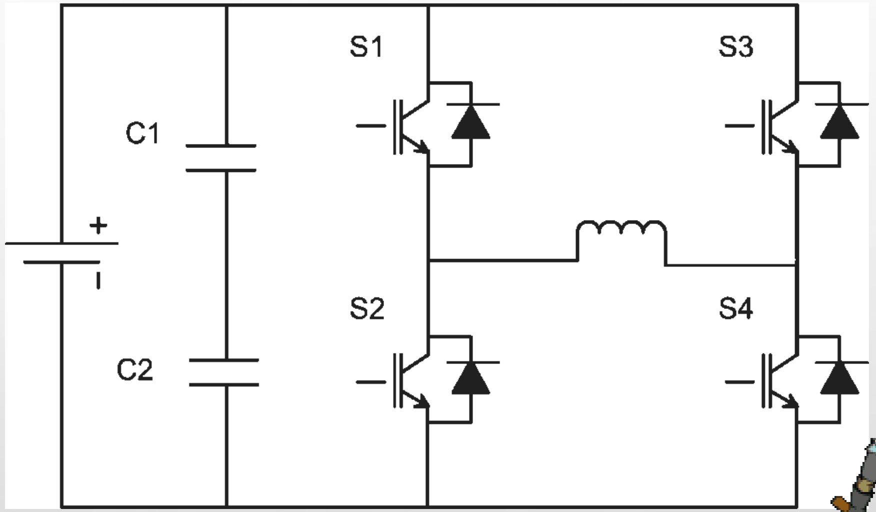
Switching conditions				Output Voltage (v_{AO})
S_{11}	S_{12}	S_{13}	S_{14}	
ON	OFF	OFF	ON	$\frac{V_{dc}}{2}$
OFF	ON	OFF	ON	0
ON	OFF	ON	OFF	0
OFF	ON	ON	OFF	$-\frac{V_{dc}}{2}$

Multilevel Inverters with Open-end Winding Induction Motor

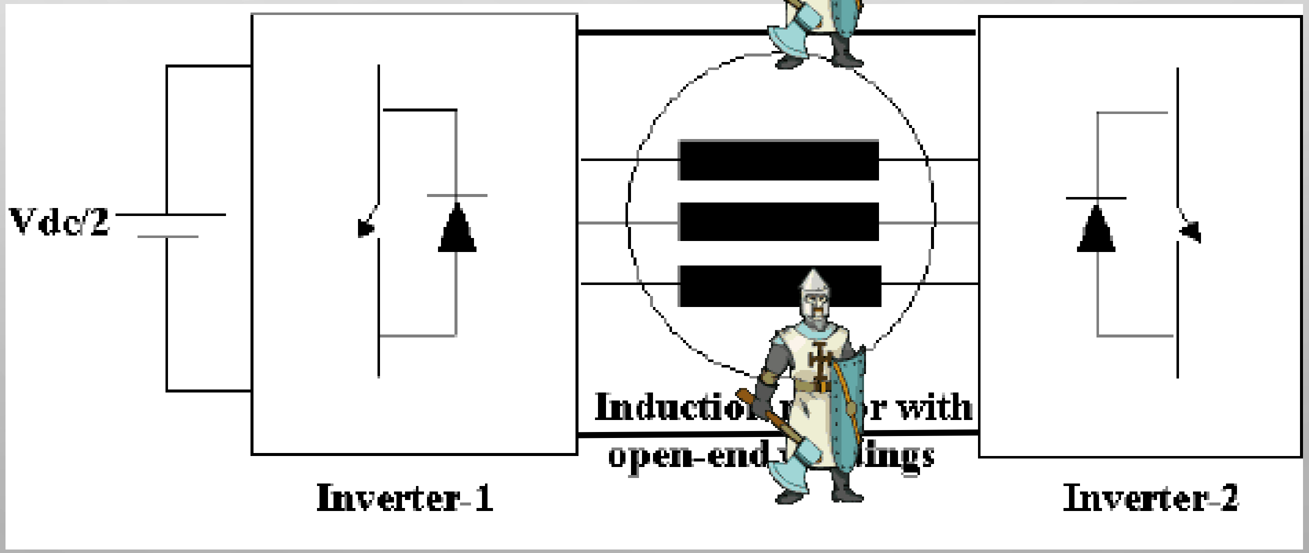




Multilevel Inverters with Open-end Winding Induction Motor



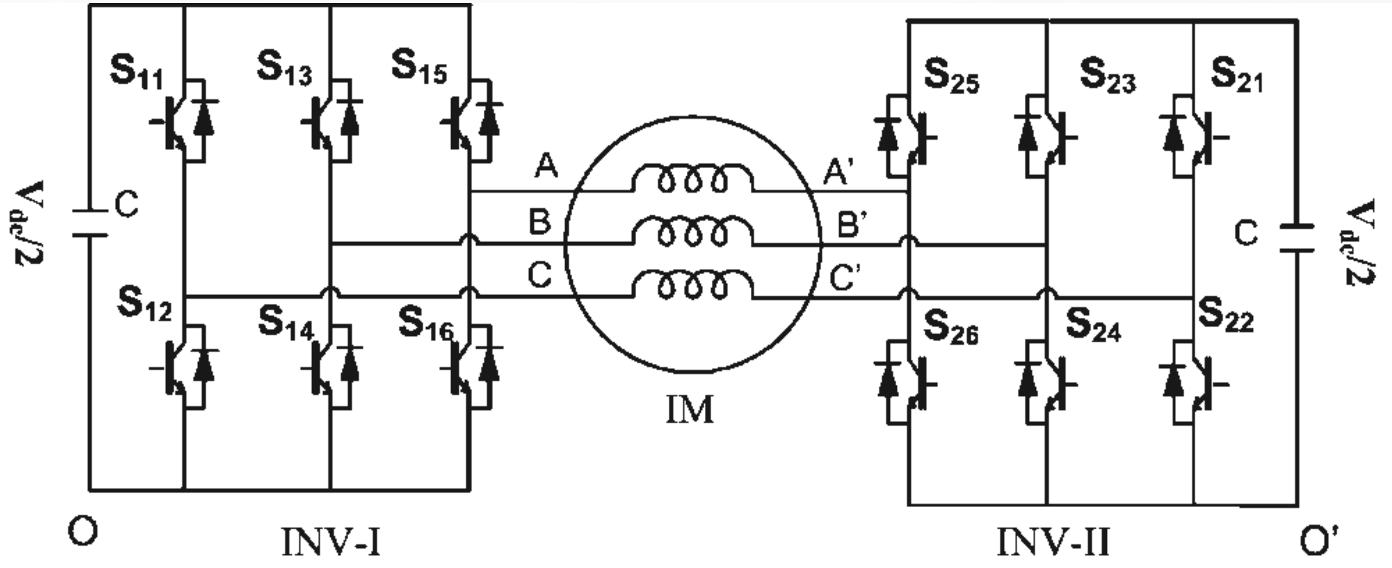
Switching condition				Output voltage
S1	S2	S3	S4	
ON	OFF	OFF	ON	Vdc/2
ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	-Vdc/2

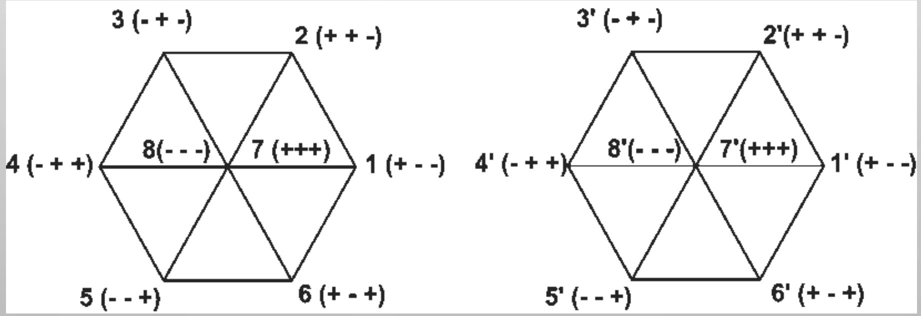


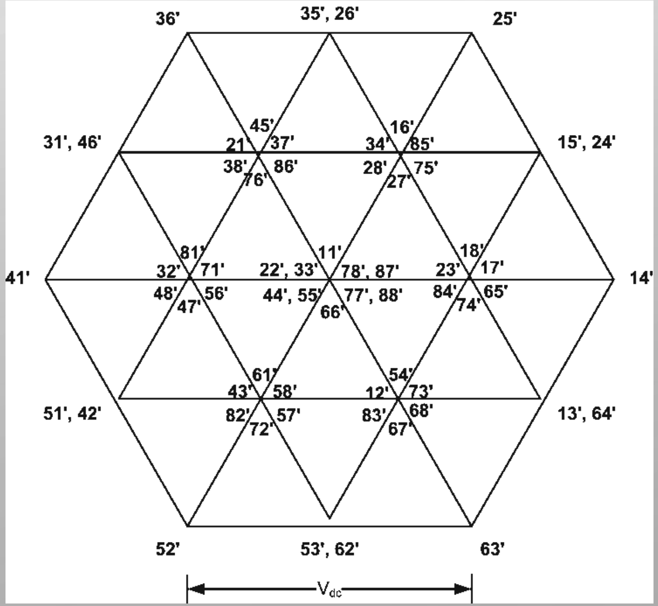
Problem with com mode currents

How it can be solved

Three-level inverter topology



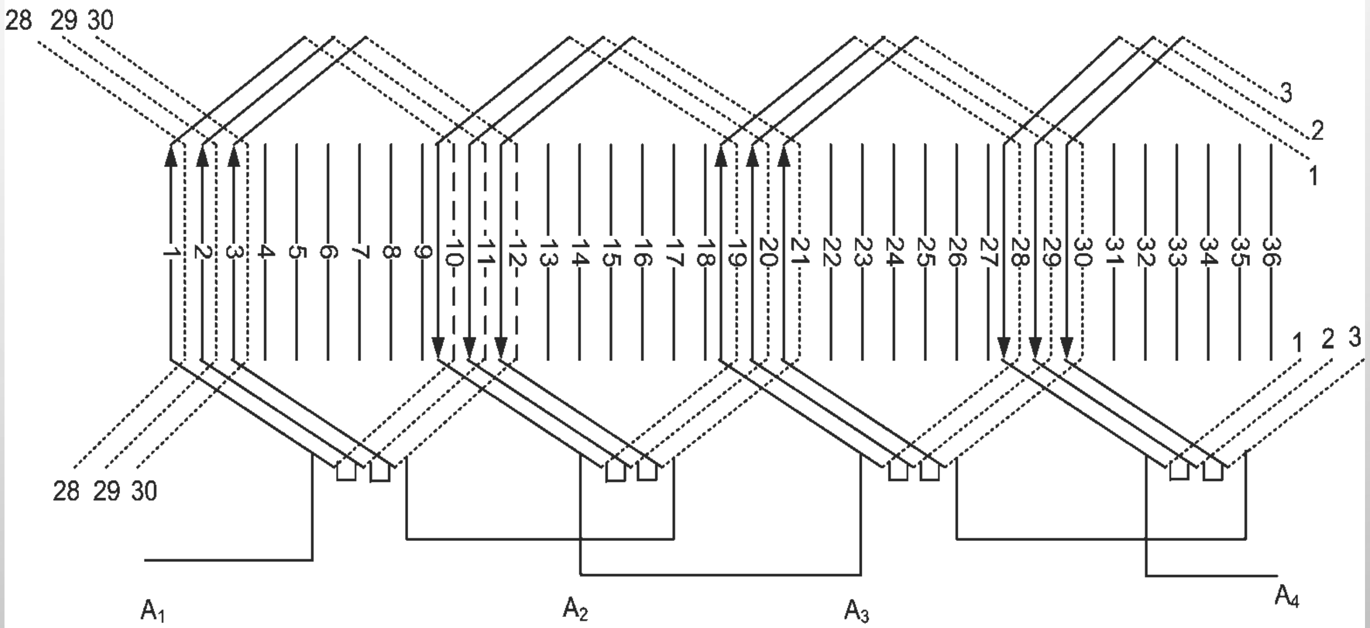




Space vector diagram

Induction machine stator winding arrangement

- Stator winding of an induction machine is an arrangement of conductors in the machine slots to produce nearly sinusoidal air gap MMF

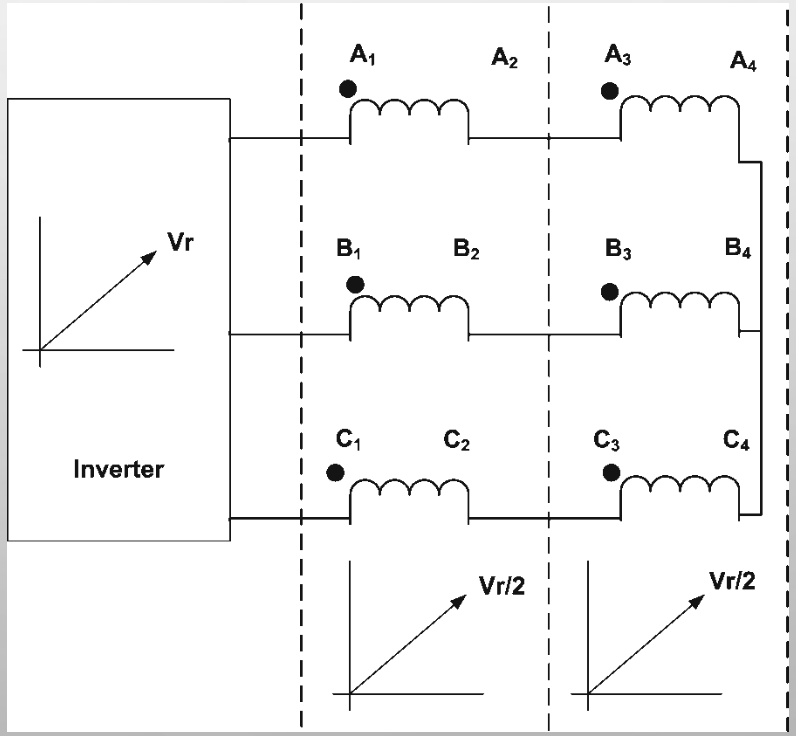


Four pole induction motor stator winding (full pitch) diagram

- The conductors in the slots 1 to 3 and 19 to 21 should have the same voltage profile to produce identical magnetic poles
- Similarly the conductor in the slots 10 to 12 and 28 to 30 should have the same voltage profile

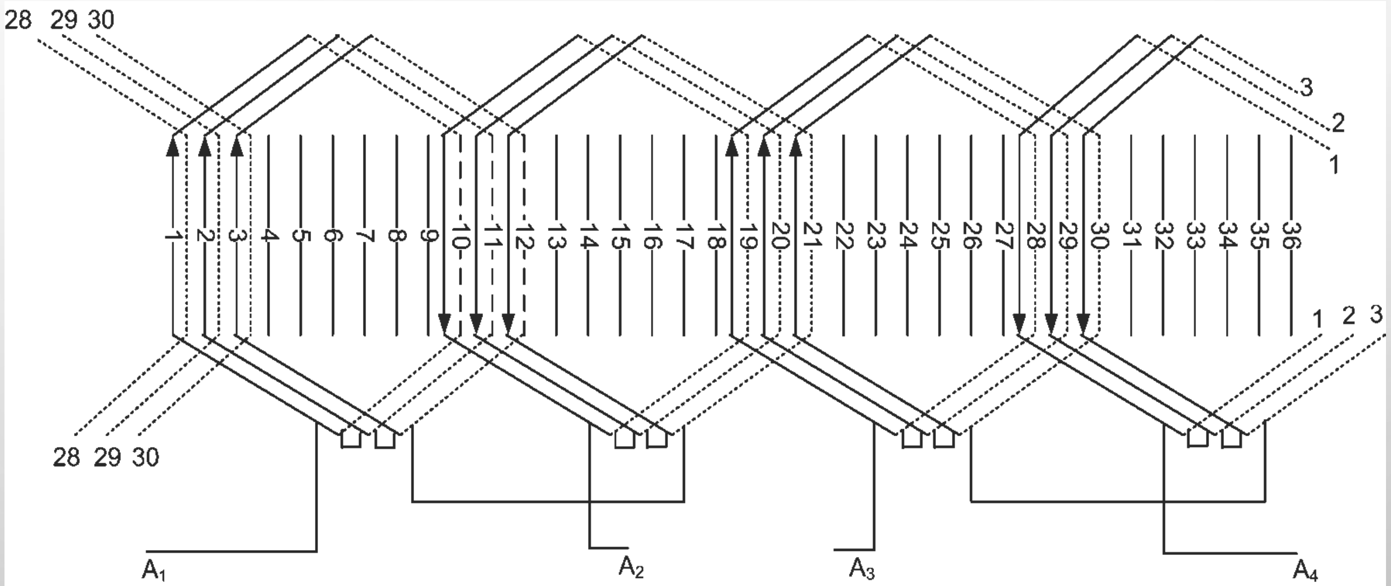
➢In a four pole induction motor, two sets of identical voltage profile coils will be present in the total phase winding, at a phase displacement of 360° (electrical)

➢The identical voltage profile winding coils (or pole pair winding coils) in the stator winding will equally share the applied voltage vector

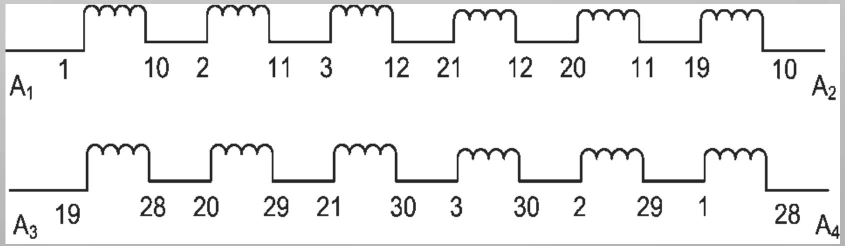


Voltage vector distribution in the four pole induction machine winding

➢These identical voltage profile winding coils can be disconnected from a conventional four pole induction machine without any design change

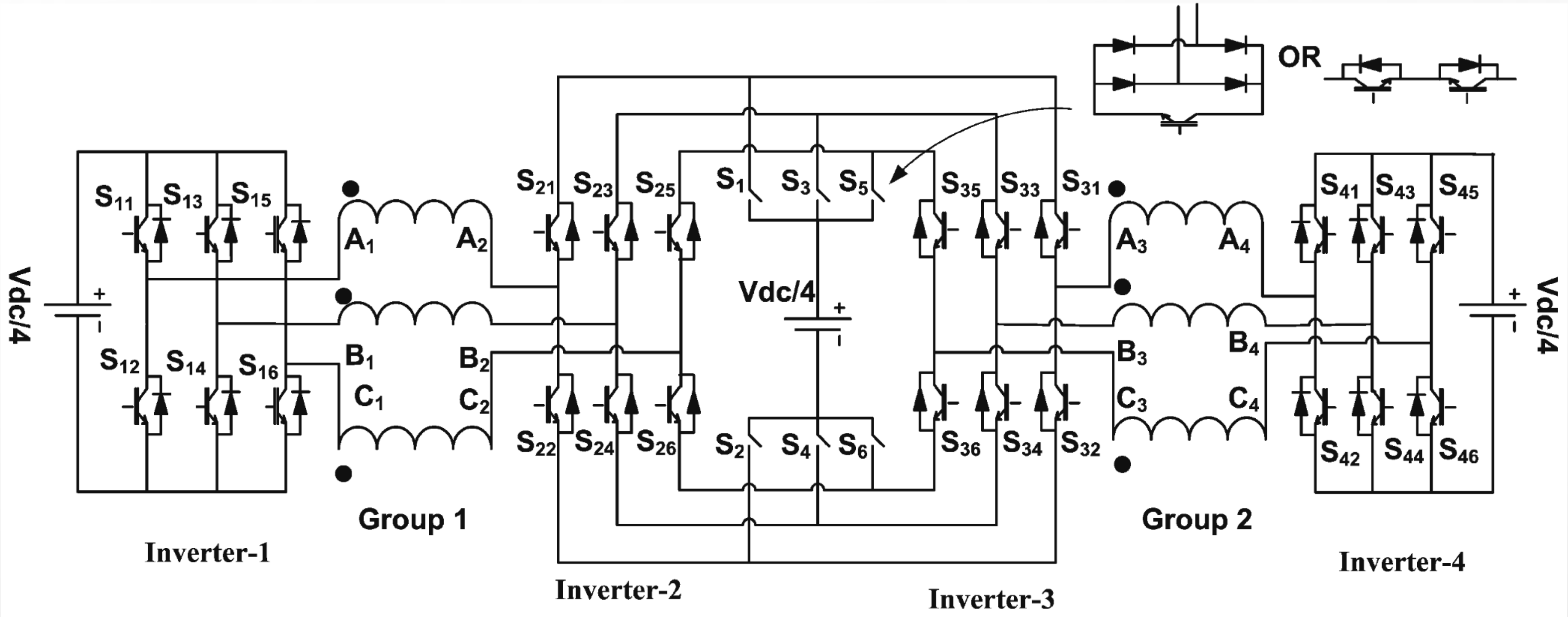


Modified four pole induction motor stator winding diagram



Coil connection after the identical pole pair winding disconnection

Proposed Five-level Inverter Power circuit

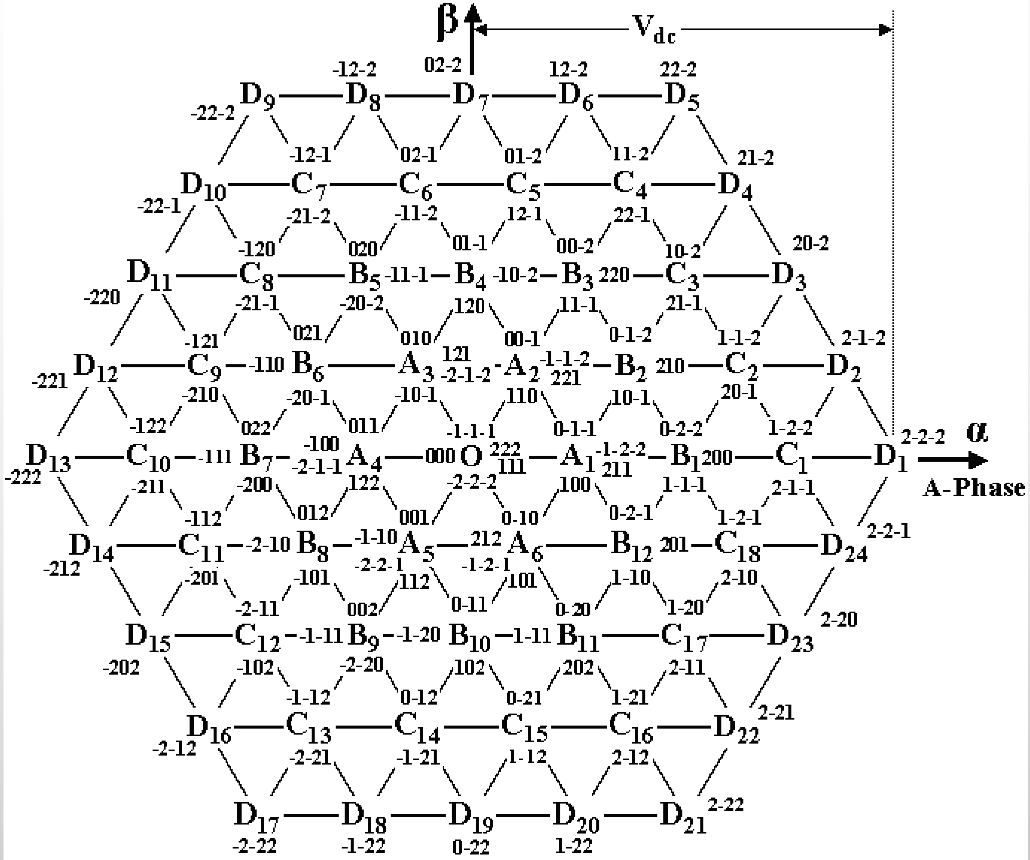


➢The advantages of the open-end winding structure along with identical voltage profile winding coils for a four pole induction motor are effectively utilized to realize multilevel structures using conventional two-level inverters

All switching combinations for the five voltage levels for a-phase

Voltage magnitude (level)	S_{11}	S_{21}	S_{31}	S_{41}
$+V_{dc}/2$ (2)	ON	OFF	ON	OFF
$+V_{dc}/4$ (1)	ON	OFF	OFF	OFF
OFF	OFF	ON	OFF	
ON	ON	ON	OFF	
ON	OFF	ON	ON	
0 (0)	OFF	OFF	OFF	OFF
OFF	OFF	ON	ON	
ON	ON	OFF	OFF	
ON	ON	ON	ON	
ON	OFF	OFF	ON	
OFF	ON	ON	OFF	
$-V_{dc}/4$ (-1)	OFF	OFF	OFF	ON
OFF	ON	OFF	OFF	
ON	ON	OFF	ON	
OFF	ON	ON	ON	
$-V_{dc}/2$ (-2)	OFF	ON	OFF	ON

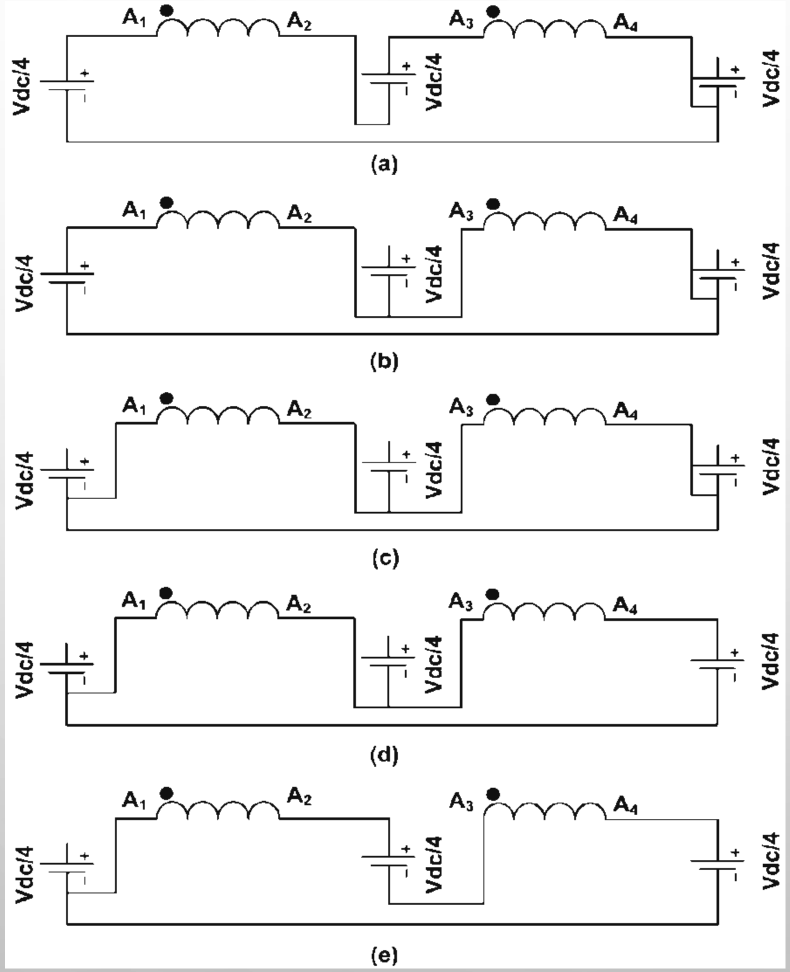
➢Presently, the bi-directional switches S_1 to S_6 , in the power circuit, are assumed to be shorted



Voltage space vector locations for a Five-level inverter

- Note that each voltage level can be realized in a number of ways

Schematic of possible voltage levels across the A-phase winding



Voltage level at $V_{dc}/2$

Voltage level at $V_{dc}/4$

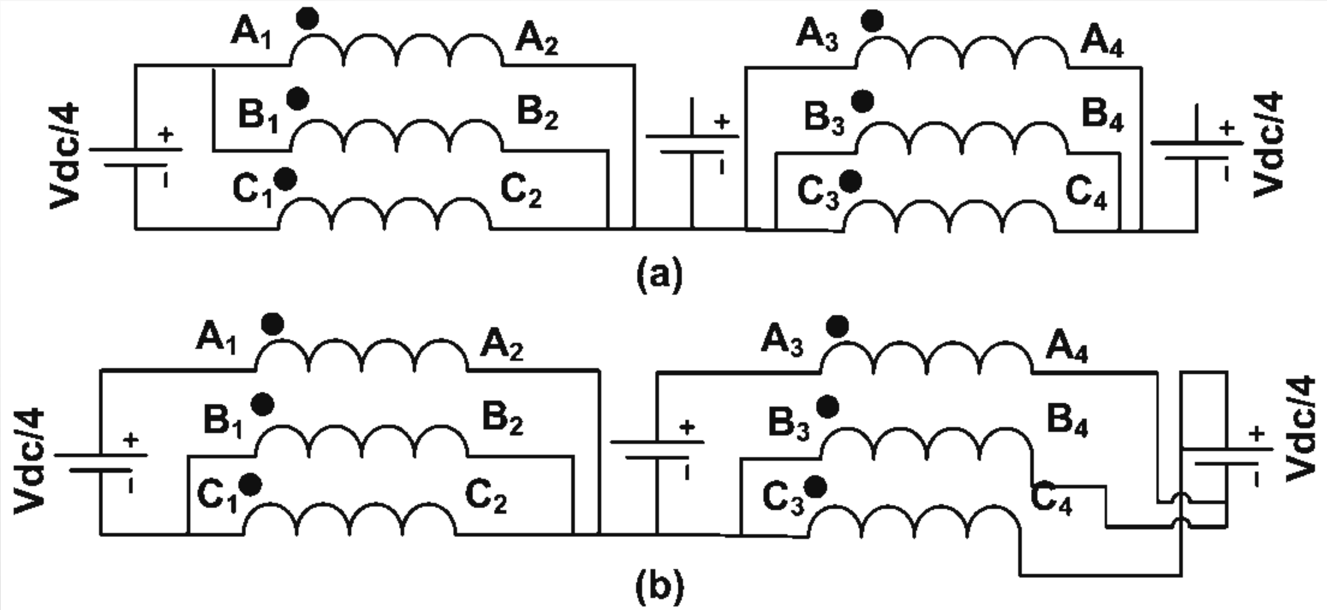
Voltage level at 0

Voltage level at $-V_{dc}/4$

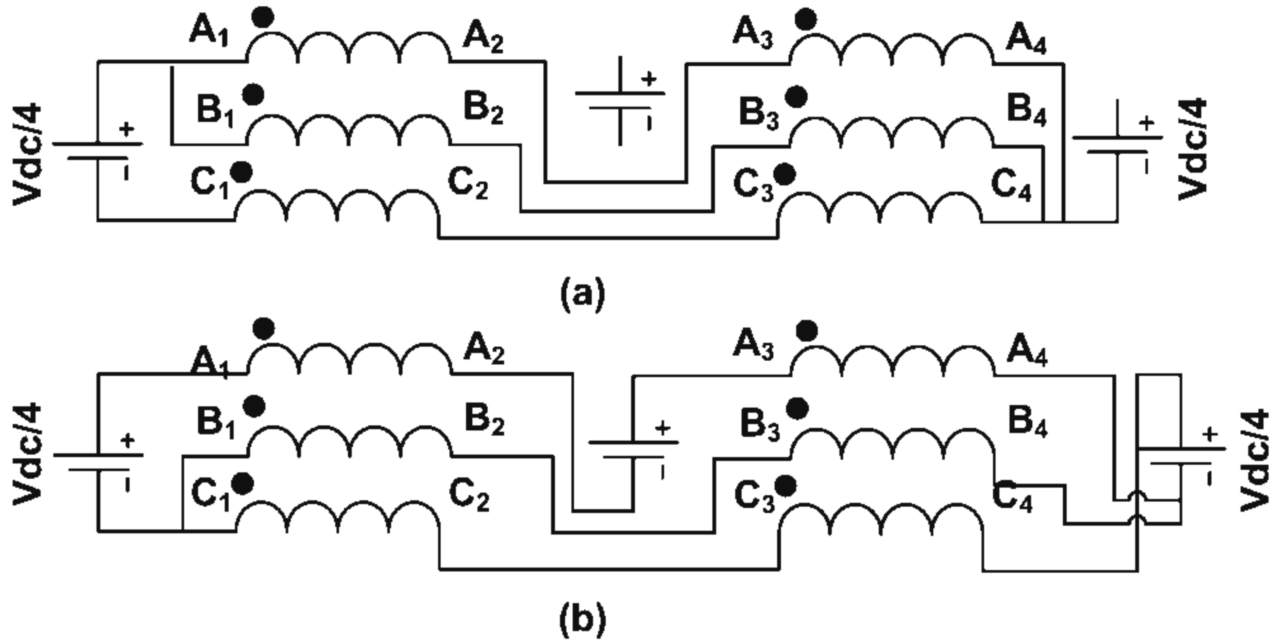
Voltage level at $-V_{dc}/2$

- As mentioned above turning on the bidirectional switches (S_1 to S_6) permanently will cause a short circuit at the middle of motor phase windings

➢It will create an unequal voltage sharing between the same winding groups and this is explained using with switching state combinations 110 and 20-1



(a)Phase winding connection to the voltage sources for switching state 110
(b) Phase winding connection to the voltage sources for switching state 20-1



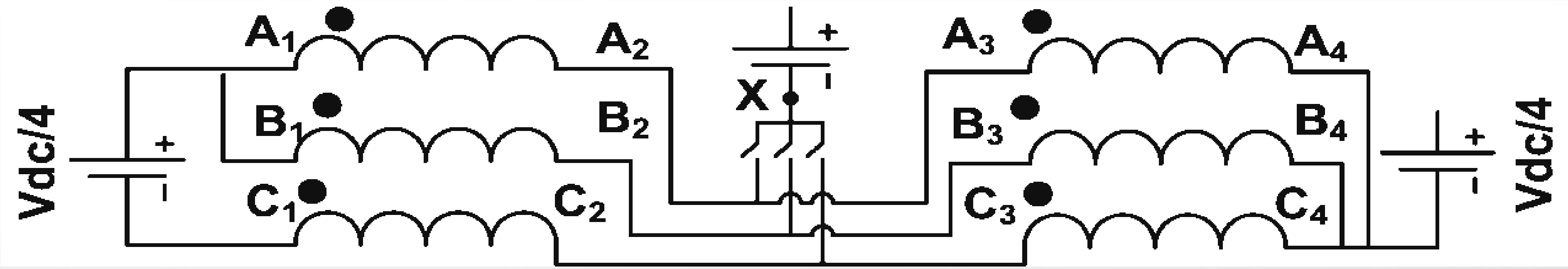
(a) Phase winding connection to the voltage sources with equal voltage distribution across the phase winding groups for switching state 110 using the bidirectional switches. (b) Phase winding connection to the voltage sources with equal voltage distribution across the phase winding groups for switching state 20-1 using the bidirectional switches

➢Based on the above considerations it is not possible to realize all the switching combinations presented in the above table

➢The possible switching combinations for the proposed topology with appropriately selecting the bidirectional switches for the A-phase are presented bellow

Voltage magnitude (level)	S_{11}	S_{21}	S_{31}	S_{41}	S_1	S_2
$+V_{dc}/2$ (2)	ON	OFF	ON	OFF	ON	ON
$+V_{dc}/4$ (1)	ON	OFF	OFF	OFF	OFF	OFF
ON	ON	ON	OFF	OFF	OFF	
0 (0)	OFF	OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	OFF	OFF	
ON	OFF	OFF	ON	OFF	OFF	
OFF	ON	ON	OFF	OFF	OFF	
$-V_{dc}/4$ (-1)	OFF	OFF	OFF	ON	OFF	OFF

voltage rating of the bidirectional switches



Phase winding connection to the voltage sources for switching state 22-2, with bi-directional switches

- the voltage equation for the loop (using Kirchhoff's voltage Law) ($B_1 \rightarrow B_2 \rightarrow X \rightarrow C_2 \rightarrow C_1 \rightarrow B_1$)

$$\frac{V_{dc}}{4} - \frac{e_b}{2} + \frac{e_c}{2} + 2 * V_s = 0 \quad \longrightarrow \quad V_s = -\frac{1}{2}\left(\frac{V_{dc}}{4} - \left(\frac{e_b}{2} - \frac{e_c}{2}\right)\right)$$

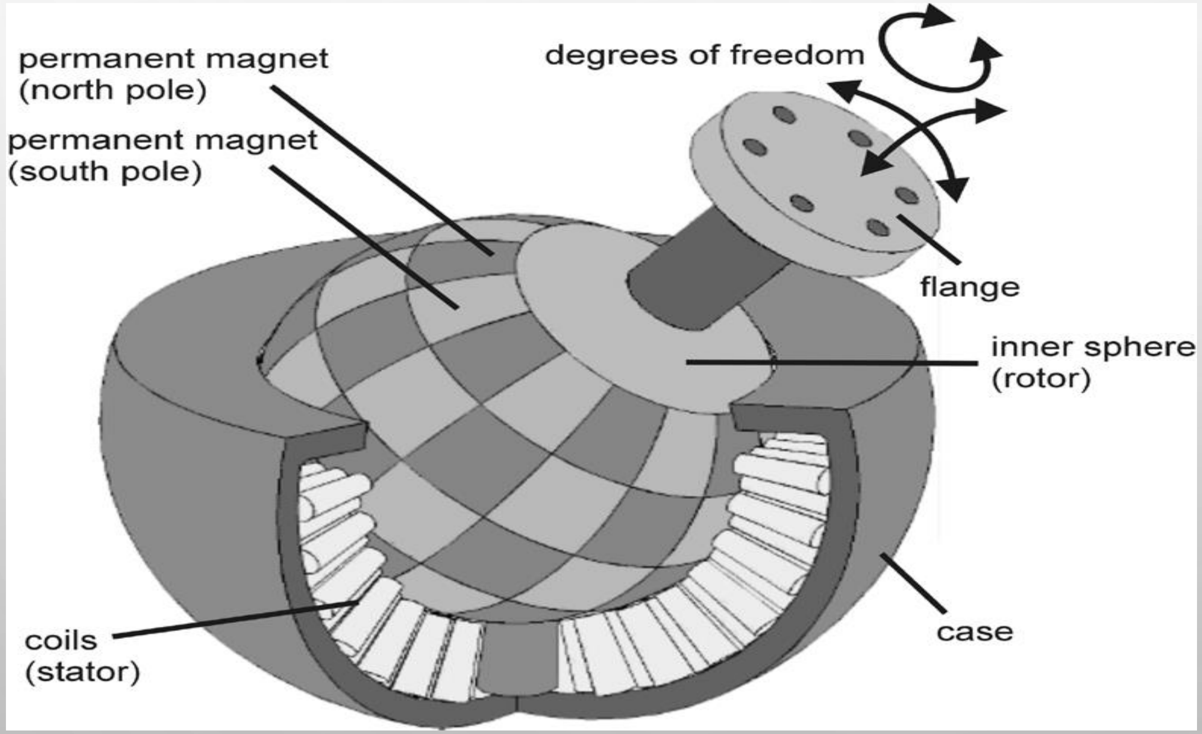
- The maximum voltage across the switch is half the voltage difference between $V_{dc}/4$ and the difference between the back emf's of two phases
- Maximum voltage appears across the bidirectional switches is $V_{dc}/8$

Comparison between the proposed topology and conventional topologies

	NPC Topology	Flying capacitor topology	H-bridge topology	Proposed topology
Switches (with a voltage rating of $V_{dc}/4$)	24	24	24	24
Clamping diodes	Voltage rating of $3*V_{dc}/4$	6	0	0
$V_{dc}/2$	6	0	0	0
$V_{dc}/4$	6	0	0	0
Isolated voltage sources (voltage magnitude)	1^{*} (V_{dc})	1^{*} (V_{dc})	6 ($V_{dc}/4$)	3 ($V_{dc}/4$)
Number of capacitor banks (with a voltage rating of $V_{dc}/4$)	4	18	0	0
Bi-directional switches (voltage rating)	0	0	0	6 ($V_{dc}/8$)

Recent developments in Small Power Special machines

96 phase Spherical Machine With Variable Pole Pitch for robotic application



- **three degrees of freedom in motion**
- **motor consists of a rotor sphere with permanent magnets and an outer stator core casing with 96 stator poles and windings.**
- **The currents of the stator coils have to be controlled individually because the pole pitch can vary continuously during operation**

Klemens Kahlen, Ingo Voss, Christian Priebe, Rik W. De Doncker. 2004.

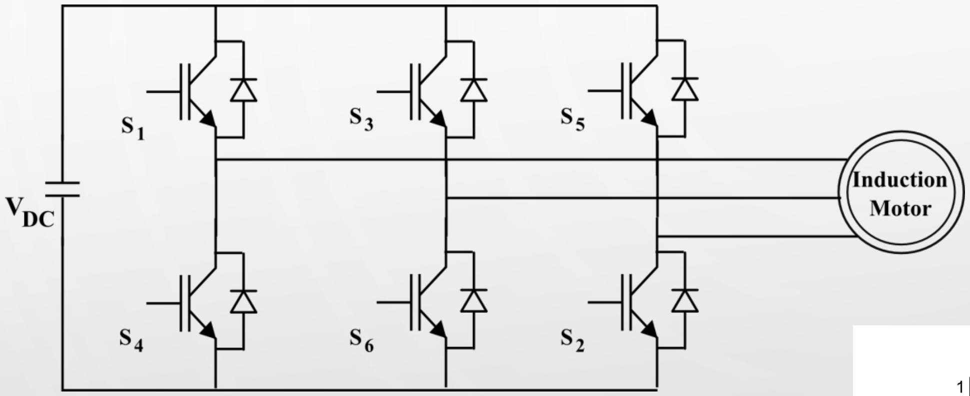
Special machines for High Power Applications

- **Electric ship propulsion**
- **Traction systems**
- **More electric aircraft**

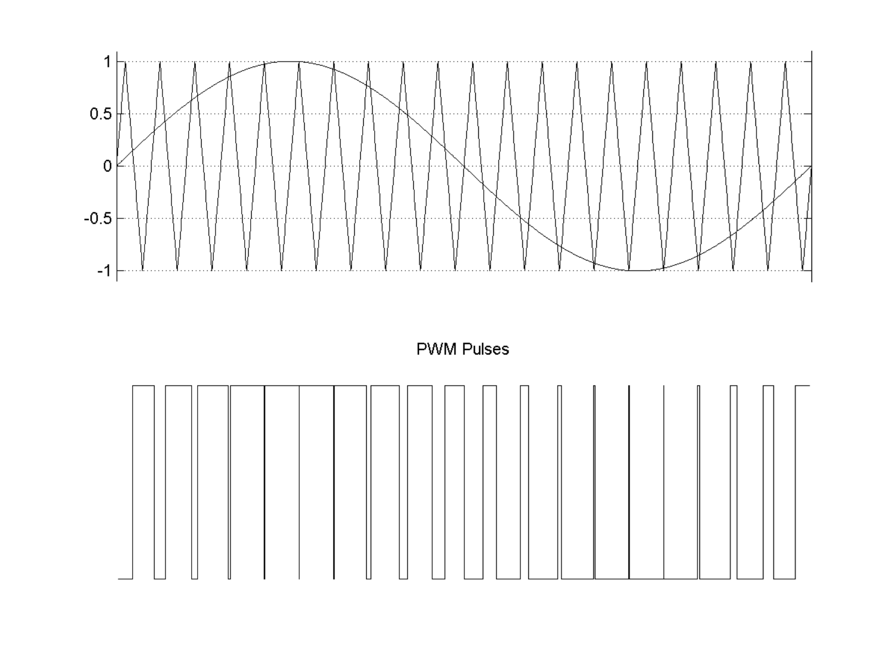
Application where handling high power density , fault tolerance and efficiency are of major concern.

PWM SWITCHING SCHEMES

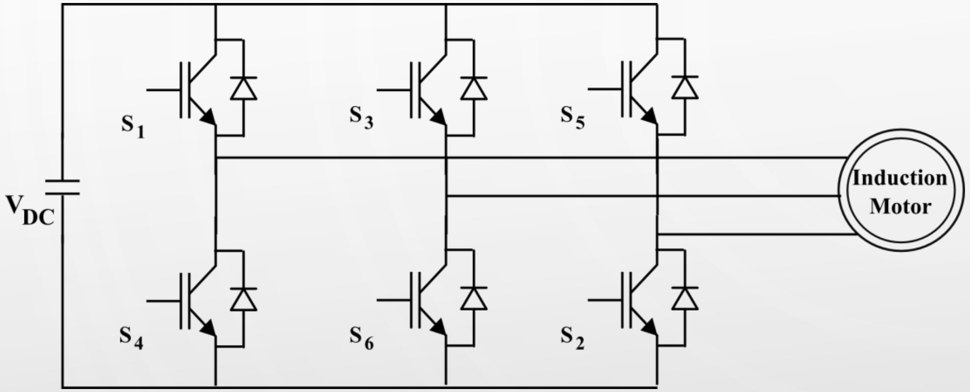
Sine-triangle PWM



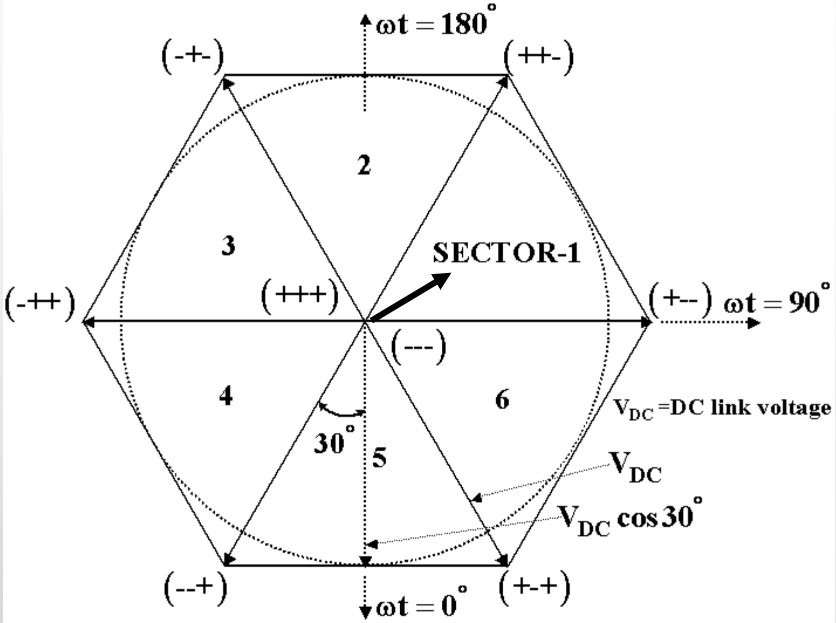
Two-level Voltage Source Inverter



SVPWM for Two-level Inverter



Two-level Voltage Source Inverter



Voltage space phasor vector locations

Where, the space vector V_r constituted by the pole voltages $v_{AO,}$ v_{BO} and v_{CO} is defined as:

$$V_s = v_{AO} + v_{BO}e^{j120^o} + v_{CO}e^{j240^o}$$

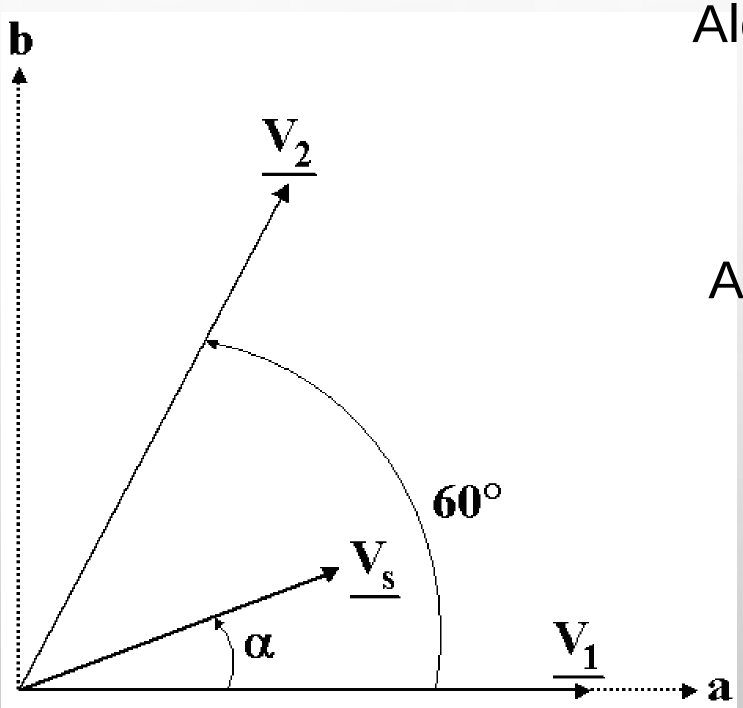
Voltage space vector

$$f_{qdo} = K_s * f_{abc}$$

$$K_s = \frac{2}{3}\begin{pmatrix} \cos\theta & \cos\left(\theta - {}^{2*\pi}\!/_{3}\right) & \cos\left(\theta + {}^{2*\pi}\!/_{3}\right) \\ \sin\theta & \sin\left(\theta - {}^{2*\pi}\!/_{3}\right) & \sin\left(\theta + {}^{2*\pi}\!/_{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}$$

$$\mathrm{V_s} = V_q + jV_d$$

SVPWM for Two-level Inverter



Along axis-a:

$$\underline{V_1}T_1 + \left(\underline{V_2}\cos 60\right)T_2 = T_s\underline{V_s}\cos\alpha$$

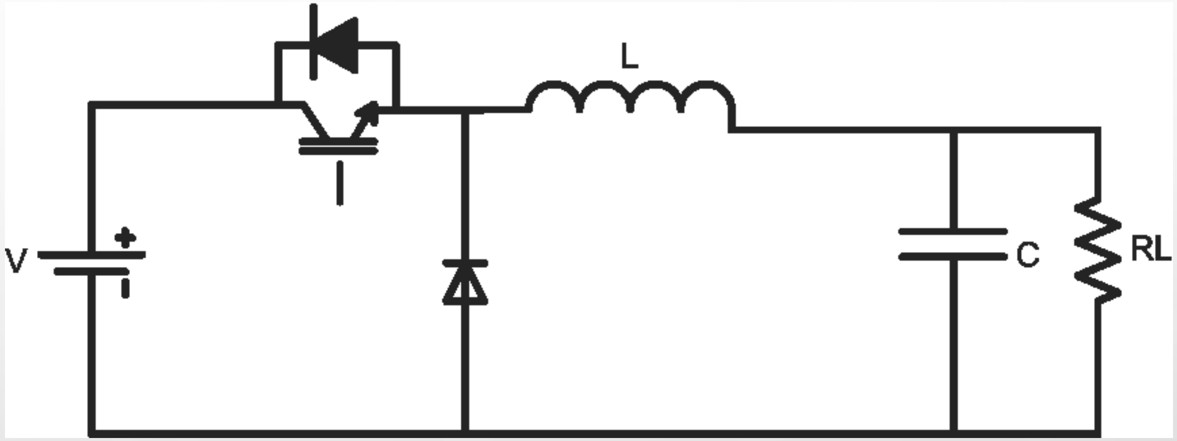
Along axis-b:

$$0 + \left(\underline{V_2}\sin 60\right)T_2 = T_s\underline{V_s}\sin\alpha$$

$$T_1 = T_s\frac{\underline{V_s}}{V_{DC}}\frac{\sin(60-\alpha)}{\sin 60}$$

$$T_2 = T_s\frac{\underline{V_s}}{V_{DC}}\frac{\sin\alpha}{\sin 60}$$

$$T_0 = T_s - \left(T_1 + T_2\right)$$



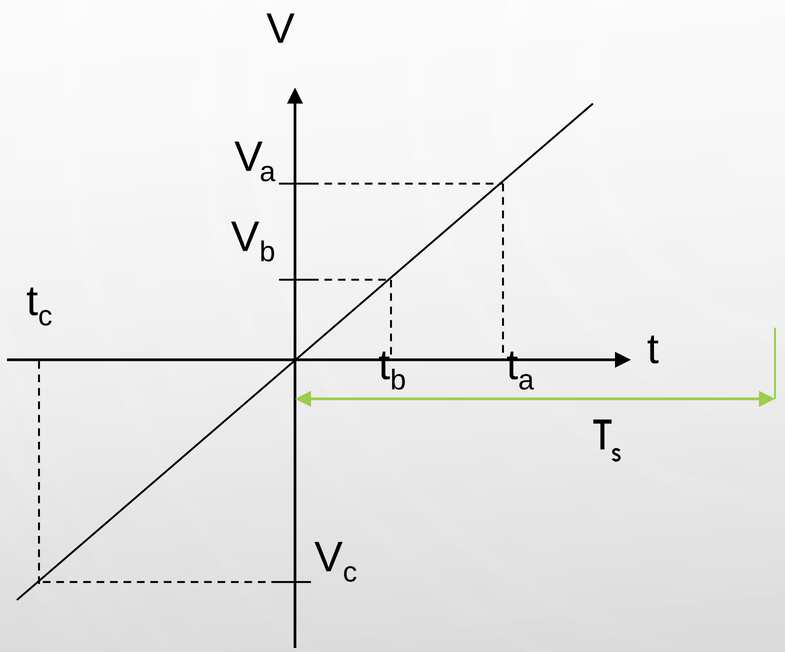
Buck Converter

$$V_o = d * V_s$$

Where

$$d = \frac{t_{on}}{T_s}$$

Space Vector PWM



$$t_{as} = t_a + T_{offset}$$

$$t_{bs} = t_b + T_{offset}$$

$$t_{cs} = t_c + T_{offset}$$

$$T_{offset} = -t_{min} + t_0/2$$

$$t_{as} = t_a - t_{min} + t_0/2$$

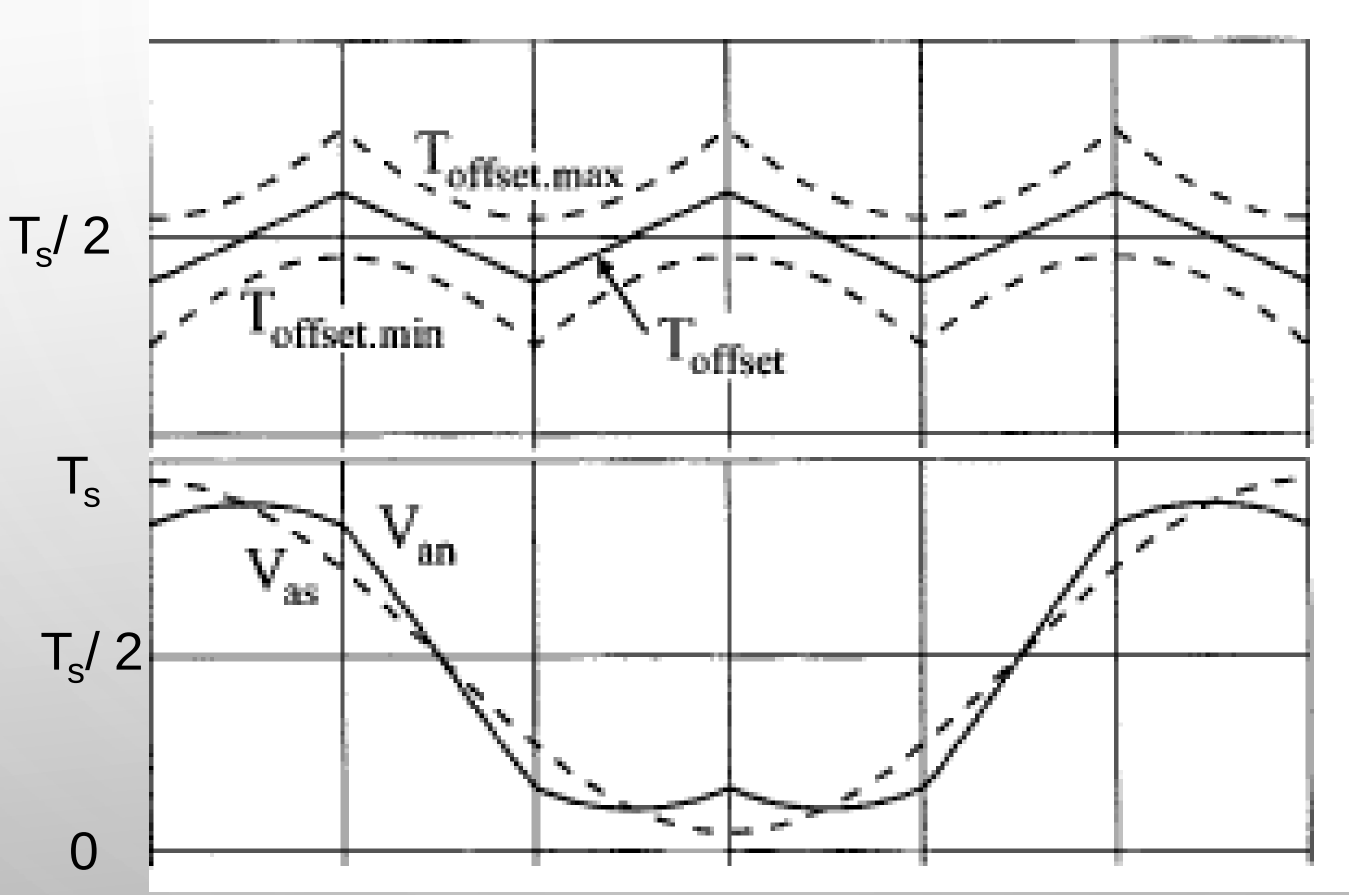
$$t_{bs} = t_b - t_{min} + t_0/2$$

$$t_{cs} = t_c - t_{min} + t_0/2$$

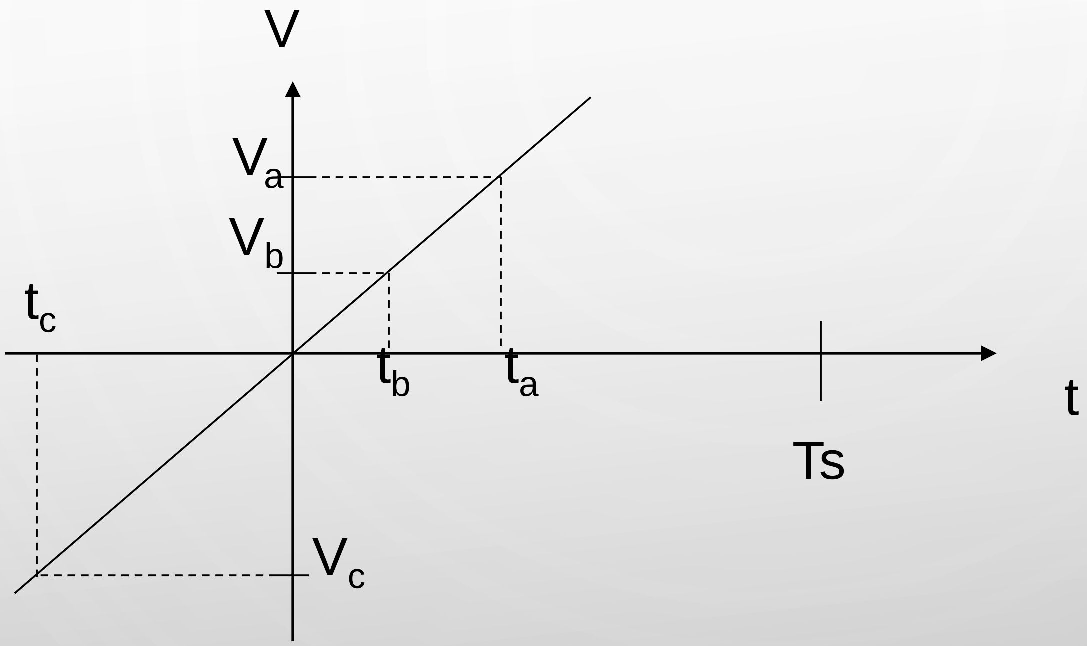
$$t_{as} = t_a - t_{min} + 1/2\left[T_s - \left(t_{max} - t_{min}\right)\right]$$

$$t_{as} = t_a + 1/2\left[T_s - \left(t_{max} + t_{min}\right)\right]$$

Offset time and modulating wave



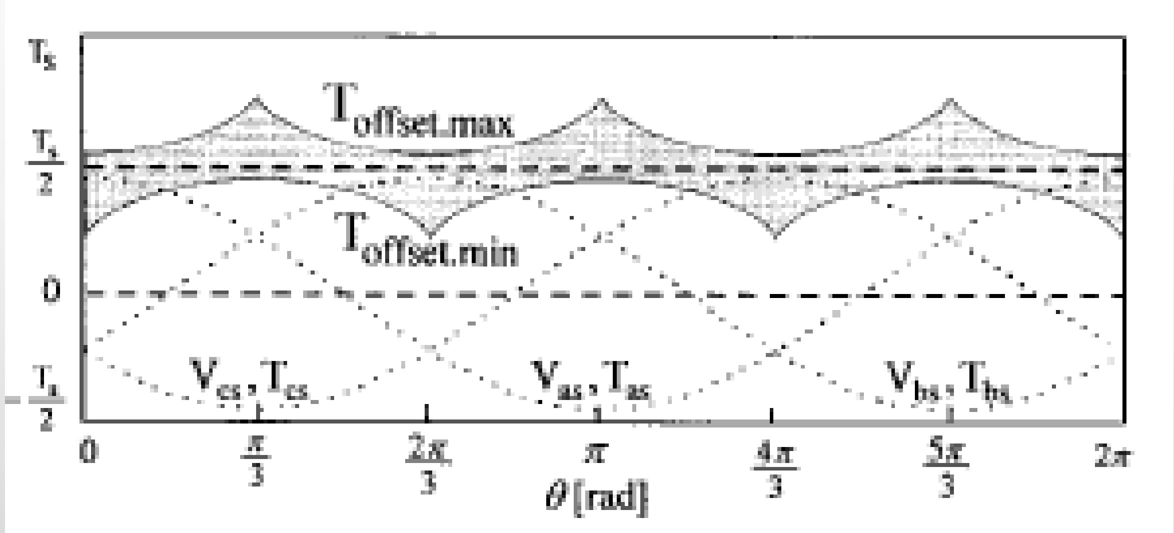
Minimum and Maximum value of offset time



$$T_{offset}(\min) = -t_{\min}$$

$$T_{offset}(\max) = T_s - t_{\max}$$

Minimum and Maximum value of offset time



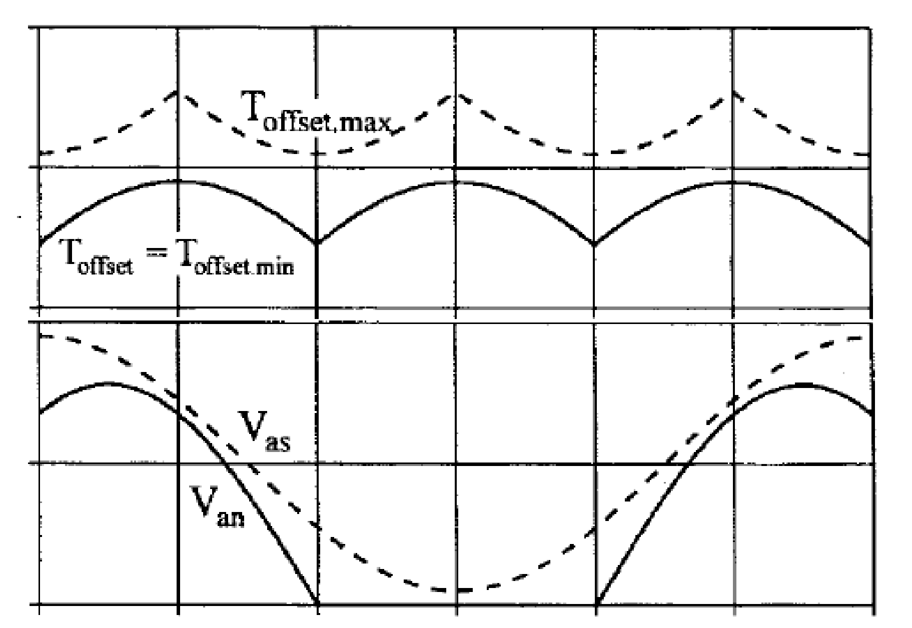
$$T_{offset}(\min) \le T_{offset} \le T_{offset}(\max)$$

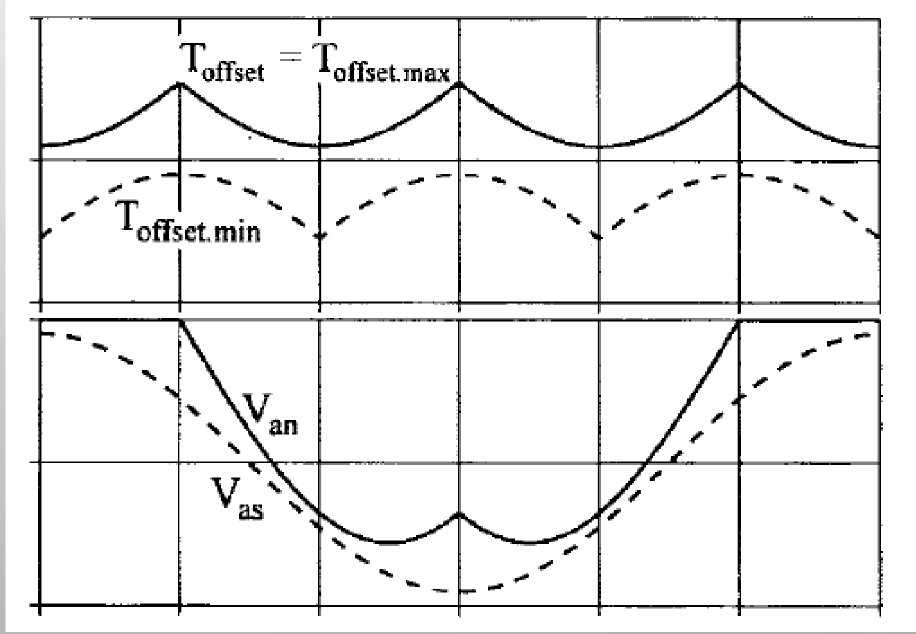
Discontinuous modulation schemes

The 120º discontinuous PWM schemes

$$T_{offset} = -t_{\min}$$

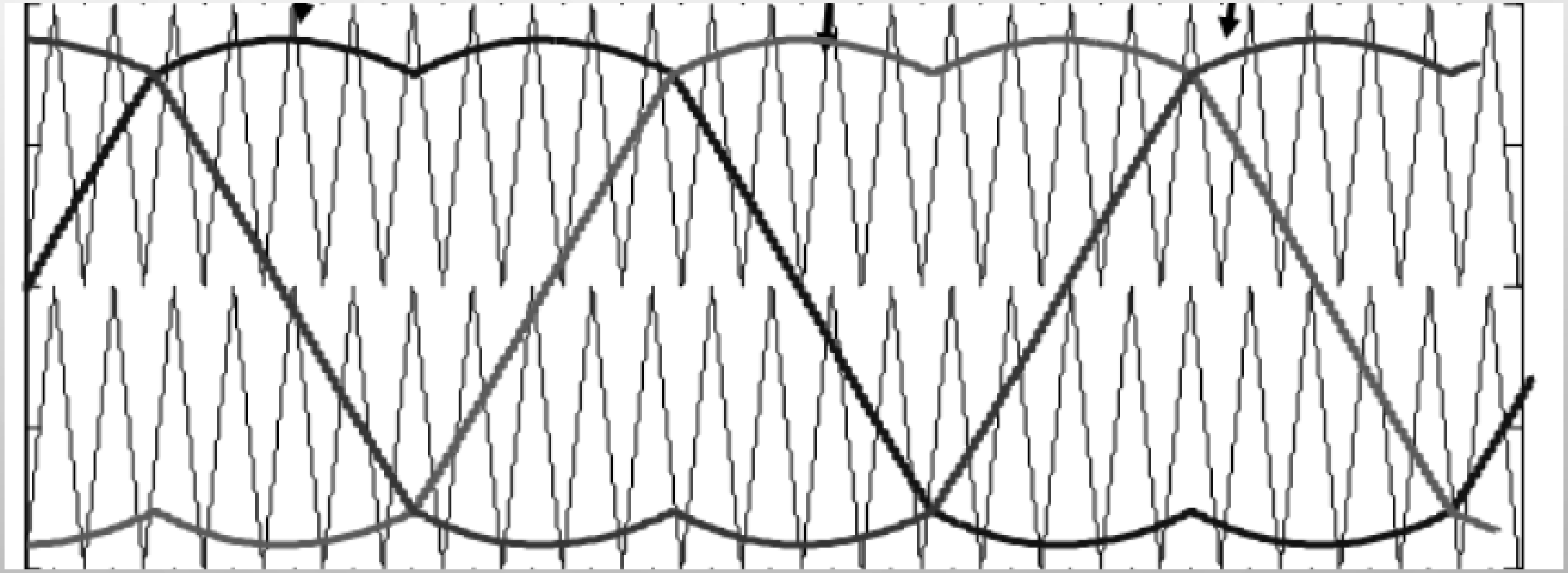
$$T_{offset} = T_s - t_{\max}$$



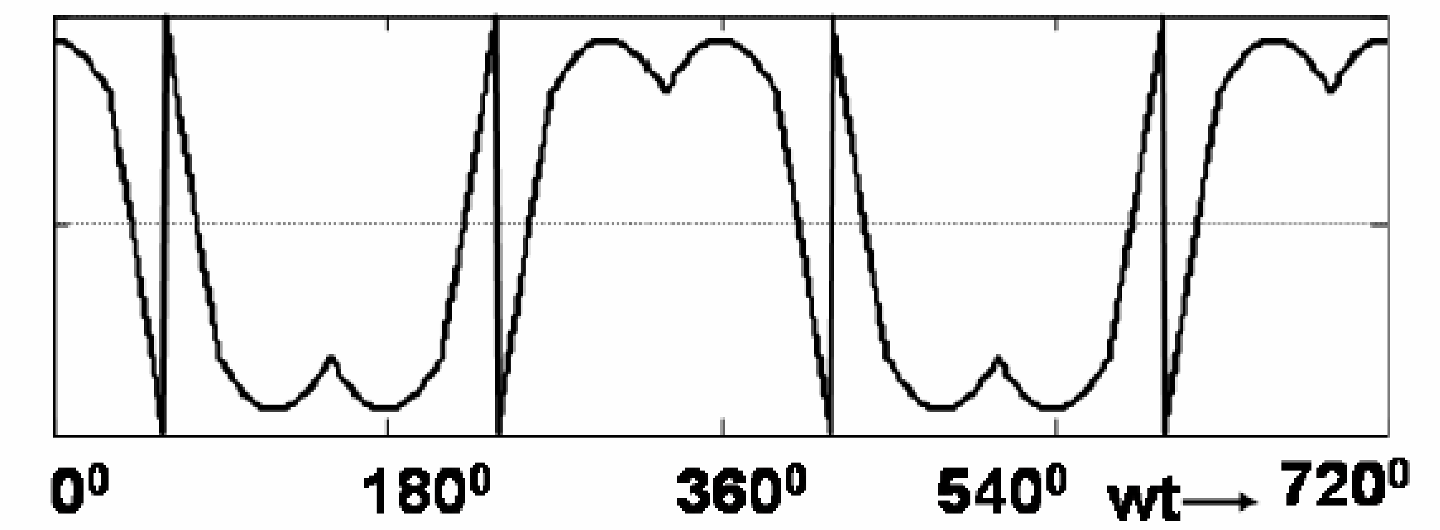


SVPWM for Three-level Inverter

Two carrier signals required to generate PWM signals for three-level inverter



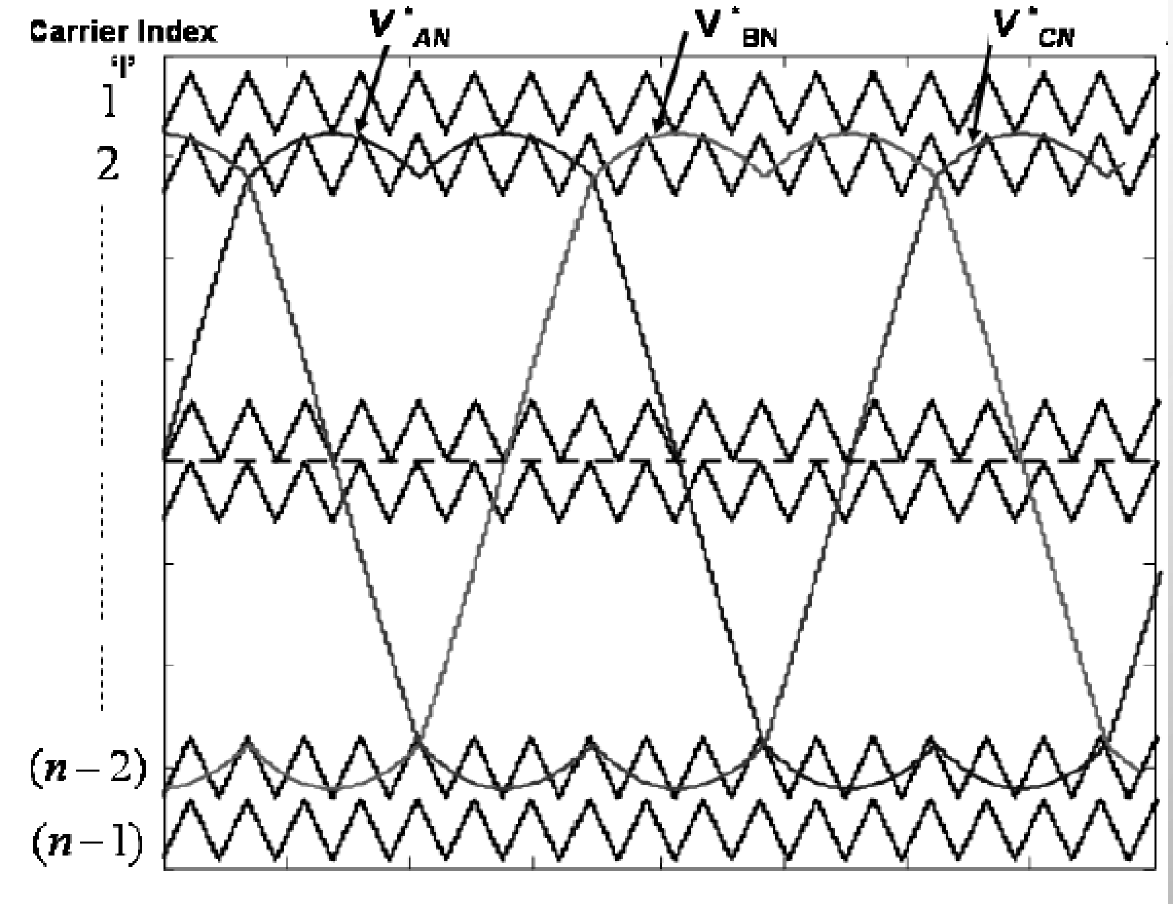
PWM signal generation with one carrier wave



PWM signals are generated with the help of level signals and compare outputs

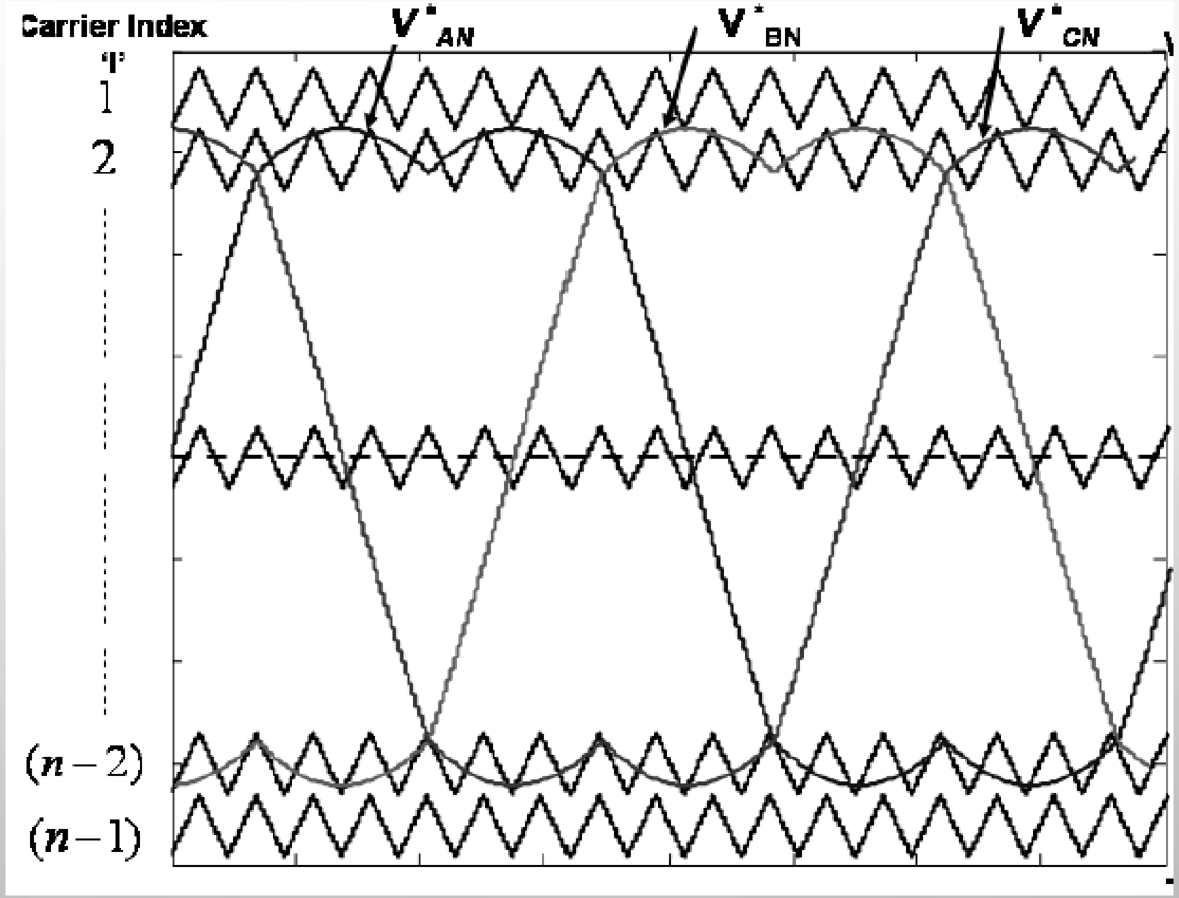
1. Compare outputs and level signals can be generate with DSP’s
2. PWM logics can be done with PAL, GAL, CPLD and FPGA’s

SVPWM for Multi-level Inverter



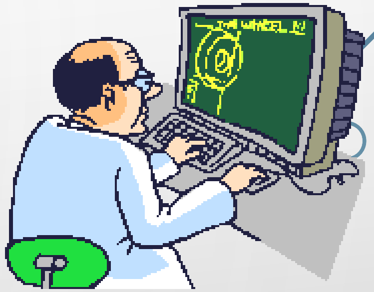
Triangular carriers and the reference signals for an '*n*' level PWM scheme where '*n*' is odd

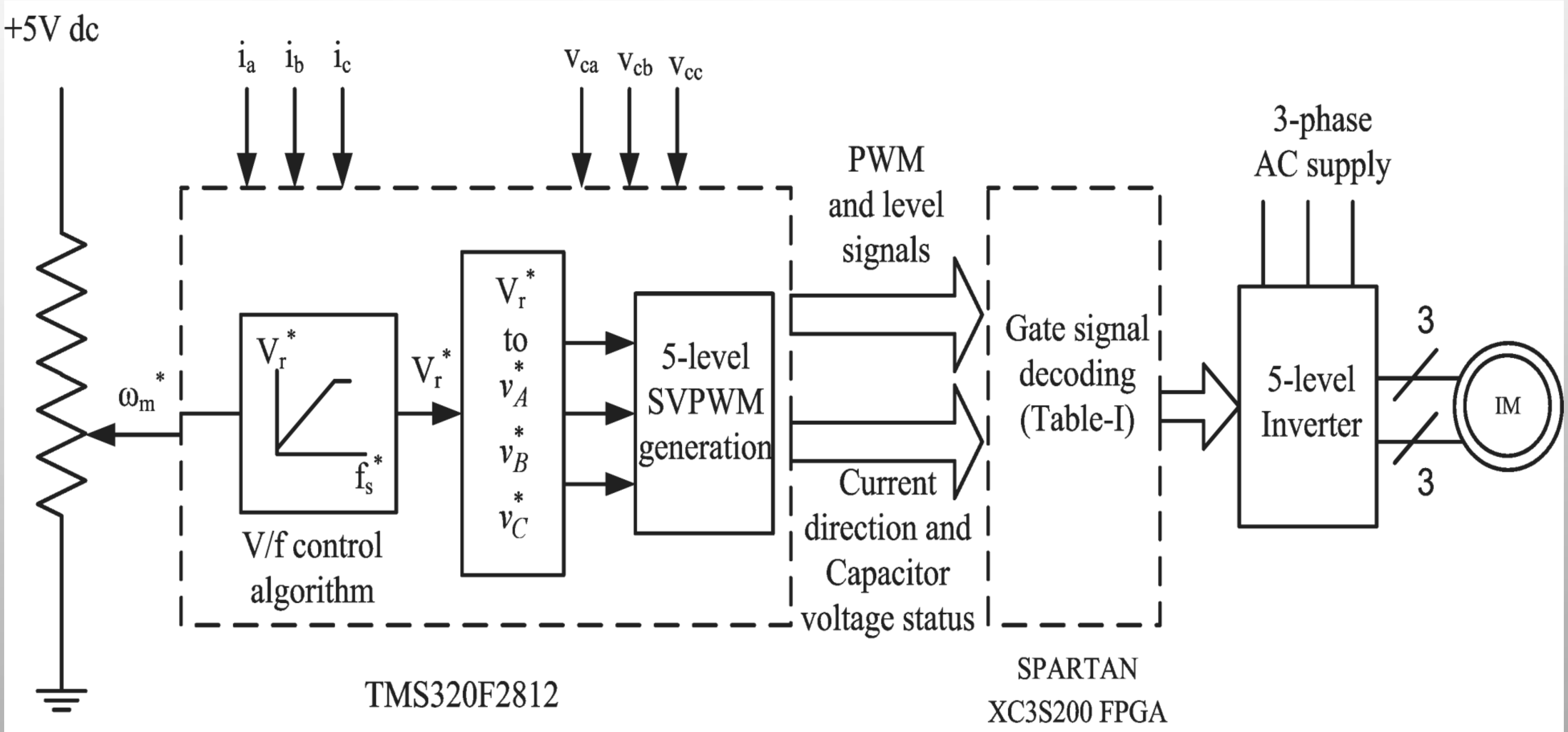
SVPWM for Multi-level Inverter



Triangular carriers and the reference signals for an '*n*' level PWM scheme where '*n*' is even

How to Implement open loop V/f controller with space vector PWM using DSP Processors





Generate V_α and V_β from the reference voltage vector using the formulas

$$V_\alpha = V_r * \cos(\emptyset)$$

$$V_\beta = V_r * \sin(\emptyset)$$

Calculate the Va, Vb and Vc references from V_α and V_β (using K^{-1} matrix)

Calculate Ta, Tb and Tc references using the above mentioned formulas and use modified kim-sul algorithm

Generation of Sine and cosine waveforms

Using Look-up tables

S.No	Angle	Sine values
1	0	0
2	360/256	0.025
256	360-(360/256)	

How to control the frequency

Frequency of sine wave can be controlled with the number of samples with fixed sampling time

How?

Number samples required = switching frequency/fundamental frequency

Number of samples to be skipped in table is proportional to the fundamental frequency

As number of samples to be skipped is proportional to the fundamental frequency

Fundamental frequency is proportional to the Voltage vector reference

So number of samples to be skipped is proportional to the Voltage vector reference

But the calculated number of samples may not be integer always…..

How to solve this?

By accounting rational numbers

Example

Number of Samples in sine wave look table is 256

Switching frequency is 2kHz and fundamental frequency is 50Hz

According the previous discussion number of samples required is 40
and number of samples to be skipped is 256/40 (i.e. 6.4)

If we Consider only 6 samples to skip, we will end up with approximately 42 samples which is equal to an fundamental frequency of 47.6

Which is not correct, So what we can do?

Use the same value of 6.4 at the time of addition i.e.

S.No.	Samples to be skipped	Number of sample to read (from starting of the table)
1	0	0
2	6.4	6
3	12.8	12
4	19.2	19
5	25.6	25
6	32	32 (Error is minimized to zero)

So use any number format to execute the above

What is the preferred number format?

To represent 256 samples 8bits are sufficient (i.e. 8MSB are sufficient to represent the integer part of offset)

Use the rest of 8LSB to take of the fractional part

If your sine table length is 512 samples than one can use 9.7 format

THANK YOU