Design of Synchronous Reference Frame phase locked loop (SRF PLL) and Sliding Goertzel Discrete Fourier Transform (SGDFT) PLL for distorted grid conditions

K.Sridharan and B.Chitti Babu, Member SMIEEE

Abstract— A converter-interfaced distributed generation (DG) system, e.g., wind power system, photovoltaic (PV) and micro-turbine-generator system, requires a fast and exact detection of phase and fundamental frequency of grid current in order to implement the control algorithm of power converters by generating reference currents signals. Moreover, a desired synchronization algorithm must detect the phase angle of the fundamental component of grid currents as fast as possible while adequately eliminating higher order harmonic components. This paper explores The overall performance of SGDFT filtering is analyzed and the obtained results are compared to Synchronous rotating reference frame (SRF) PLL method to confirm the feasibility of the study under various grid operation states such as high frequency harmonic injection .The proposed SGDFT based phase detection shows a robust phase tracking capability with fast transient response under adverse situation of the grid.

Index Terms— sliding Goertzel discrete Fourier transform (SGDFT), phase detection, distributed generation (DG), grid synchronization.

I. INTRODUCTION

As the renewable energy sources are intermittent in nature, in order to ensure safe and reliable operation of power system based on new and renewable sources at par with conventional power plants, usually power system operators should satisfy the grid code requirements such as grid stability, fault ride through, power quality improvement, grid synchronization and active/reactive power control etc [1]. Grid code requirements are generally achieved by grid-side converter based on power electronic devices. According to grid code requirements, operation capacity of grid-side converter (GSC) largely depends on the information about the phase of the grid voltage, and the control system must be capable of tracking the phase angle of grid voltage/current accurately.

Several methods have been proposed for grid synchronizing and are available in the literature, ranging from simple methods based on detection of zero-crossings of grid voltage to more advanced numerical processing of the grid voltage based on PLL measurement [2]-[4]. But, difficulties are encountered when the inverter needs to determine phase/frequency information from a weak and a distorted grid voltage. The well-established concept of Synchronous Reference Frame (SRF) PLL is inherently tracking both the grid voltage phase angle and the grid frequency for reference signal generation of control of power converters. The principal idea of phase locking is to generate a signal whose phase angle is adaptively tracking variations of the phase angle of a given signal [3] However, analog solutions provided by PLL techniques are often unsatisfactory, primarily because if the grid voltage is filtered before the phase detector, it is quite difficult to avoid introducing phase lead or lag into the filtered waveform. In order to alleviate this problem, several digital filtering techniques have been proposed. On the other hand, applications of digital signal processing (DSP) to the modern power systems have received the increase in attention for the past couple of decades. The finite impulse response (FIR) filter is one among them with great interest, because of its linear phase response that leads to accuracy in phase estimation [5]. However the method based on FIR Filtering, can also be complex to understand and implement. A new adaptive notch filtering based phase detection system is proposed in Yazdani et al for single-phase system and it shows that the proposed system is simple, robust and less complexity in digital implementation. However, transient response is sluggish especially during grid voltage/frequency variation. Brendan Peter McGrath et al, have proposed new recursive DFT filter for phase error correction for line synchronization by using time window and phase error correction method.

This paper presents an improved phase detection system for grid-interactive power converter based on Sliding Goertzel Discrete Fourier Transform (SGDFT). The proposed SGDFT based phase detection shows a robust phase tracking capability with fast transient response under adverse situation of grid. Moreover, SGDFT phase detection system is more efficient as it requires small number of operations to extract a single frequency component, thereby reducing computational complexity and simpler than DFT. The immediate advantages of the proposed sliding Goertzel DFT PLL are: frequency adaptability, full account of unbalanced conditions, high degree of immunity to disturbances and harmonics, and

Sridharan.K Assistant Professor Department of Electrical Engineering, Saveetha School of Engineering,Saveetha University, Chennai.,INDIA.
Dr.B.Chitti Babu Department of Electrical Engineering, National Institute of Technology,Nagpur,India
Corresponding author (e-mail: srimaky@yahoo.com).

structural robustness. The superior performance of proposed SGDFT phase detection system is studied and the results are obtained under different grid environment such as high harmonic injection, frequency deviation, and phase variation etc.

II. SYNCHRONOUS REFEARANCE FRAME (SRF) PLL FOR PHASE DETECTION

The basic structure of three-phase SRF PLL is illustrated in Figure 1. To obtain the phase information, the three phase (V_a,V_b and V_c) grid voltages are transformed into two phases (V_α and $V_ß$) by using *Clark's* transformation and these two phases are transfer into direct and quadrature(dq) axis by using *Park* transformation. The phase angle θ is tracked by synchronously rotating voltage space vector along *q* or *d* axis by using PI controller.

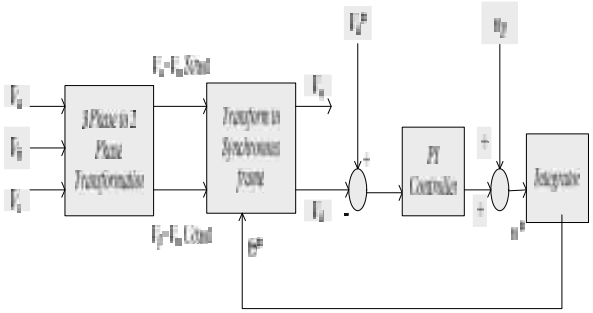


Figure 1: *Basic structure for SRF PLL system*

The corresponding voltage space vector synchronous with the q-axis is shown in Figure. 2.

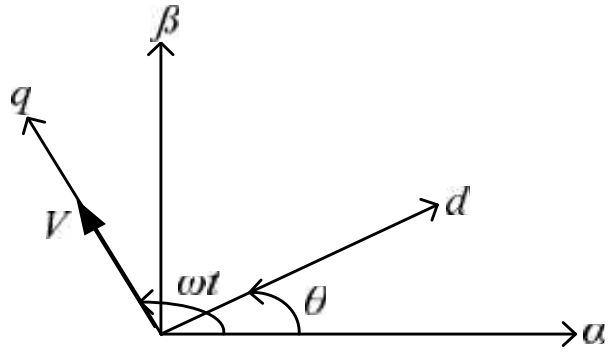


Figure 2: *Synchronous rotating reference frame*

The voltage phase vector synchronized with *q*-axis the transformation matrix is

$$T_{qd} = \begin{bmatrix} \sin^{-*} & \cos^{-*} \\ -\cos^{-*} & \sin^{-*} \end{bmatrix} \quad (1)$$

where θ^* is the estimated phase angle of the PLL system.

Carry out the transformation by using equation

$$V_{qd} = T_{qd} V_{\sim} \quad \text{,yields}$$

$$\begin{bmatrix} V_q \\ V_d \end{bmatrix} = \begin{bmatrix} \sin^{-*} & \cos^{-*} \\ -\cos^{-*} & \sin^{-*} \end{bmatrix} \begin{bmatrix} V_m \sin(^{-}) \\ V_m \cos(^{-}) \end{bmatrix} \quad (2)$$

By applying matrix multiplication and trigonometric formulas we get (3),

$$\begin{bmatrix} V_q \\ V_d \end{bmatrix} = \begin{bmatrix} V_m \cos(^{-}-^{-*}) \\ -V_m \sin(^{-}-^{-*}) \end{bmatrix} \quad (3)$$

The phase angle θ is estimated with θ^* which is integral of the estimated frequency ω*.The estimated frequency is the sum of the PI controller output and feed forward frequency ω_{ff}.The gain of the PI controller is designed that, V_d follows the reference value V_d^*=0 as in Figure 3. If V_d=0 the space vector voltage is synchronized along the *q*-axis .and estimated frequency ω* locked on the system frequency ω. So that the estimated phase angle θ^* is equals to the phase angle θ.

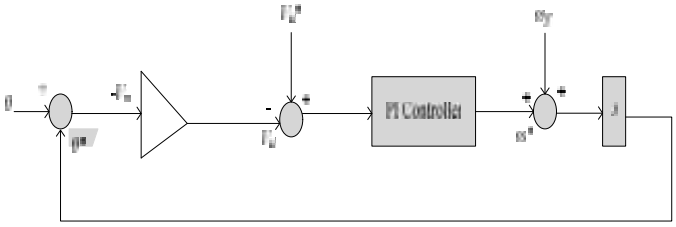


Figure 3: *Simplified system for SRF PLL.*

A. Transfer function and PI controller design

With reference to Figure.3, the transfer function for the closed loop structure of PLL composed of lag and integrating element. So the gain is given by;

$$G_{plant} = \left(\frac{1}{1+sT_s}\right)\left(\frac{1}{s}\right) \quad (4)$$

Transfer function for PI controller is,

$$G_{PI} = \left(K_p + \frac{K_i}{s}\right) = \frac{\left(K_p\right)\left(1+\frac{K_p}{K_i}s\right)}{\left(\frac{K_p}{K_i}\right)s} \quad (5)$$

$$G_{PI} = \frac{K_p\left(1+^{2}*s\right)}{^{2}*s} \quad (6)$$

where T_s is sampling period and τ is constant. The open loop transfer function for the system in Figure 3 is described as follows

$$G_{ol} = G_{plant} * G_{PI} \quad (7)$$

$$G_{ol} = \left(K_p \frac{1+s^2}{s^2}\right)\left(\frac{1}{1+sT_s}\right)\left(\frac{V_m}{s}\right) \quad (8)$$

Therefore the closed loop transfer function for the system is

$$G_{cl} = \frac{G_{ol}}{1+G_{ol}} \quad (9)$$

The relationship between s domain and *z*-domain is [6]

$$s = \frac{z-1}{T_s} \tag{10}$$

Substitute equation (10) in equation (6), we get

$$G_{PI} = K_p \frac{z-1+\frac{T_s}{2}}{z-1} \tag{11}$$

As the system is typical second order system, the gains of PI controller was estimated by using symmetrical optimum method (*SO*) [7].The idea behind the SO method is to optimize the phase margin to have its maximum value at a given cross over frequency ω_c ,

A transfer function is given by;

$$G = \frac{\mu_o^2(ks+\mu_o)}{s^2(s+k\mu_0)} \tag{12}$$

Here *k* is constant and it will be symmetrical around $\omega_c=\omega_o$. Rewrite the open loop transfer function of the SRF PLL in equation (14) yields,

$$G_{ol} = \frac{kV_m}{aT_s} \frac{\left(as+\frac{a}{2}\right)}{s^2\left(s+\frac{1}{T_s}\right)} \tag{13}$$

Where a is a Normalization factor. Comparing equation (12) and (13) gives

$$\mu_c = \frac{1}{aT_s}$$

$$^2 = a^2 T_s \tag{14}$$

$$k = \frac{1}{aV_m s}$$

These are the results for the PI regulator gains using the SO method. For a given sampling period T_s the cross over frequency can be chosen by adjusting the normalization factor a. By using these above equations, bode plot for the open-loop system is plotted and is given in figure 4. It was shown that, both the phase and magnitude curve is symmetric around the crossover frequency ($\omega_c=2*\pi*50$). The phase margin is *84.4* degrees at ω_c .

For a second order system, to measure between crossover frequency ω_c and the bandwidth ω_B for the closed loop system is approximately constant when designing the gains by considering higher phase margin which gives less oscillatory response, lower value of τ decreases the settling time and value of gain effects both phase margin and bandwidth. And therefore good value for the crossover frequency ω_c would be around the grid frequency of 50Hz that gives maximum phase margin at 50Hz. For the second order closed loop system the quotient between cross over frequency (ω_C) and bandwidth(ω_B) is approximately constant [7],

$0.6 < \omega_c/\omega_b < 0.8$

So therefore we got bandwidth $\omega_B=\omega_C/0.69=71.9$ Hz as shown in Figure.5.from that closed loop system will also have the characteristics of a low pass filter.

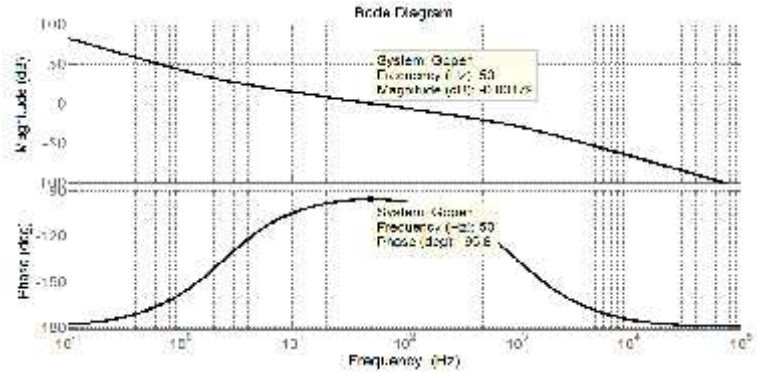


Figure 4: *Bode plot of the open-loop system. Both the phase and magnitude curve is symmetric around the crossover frequency ωc. The phase margin is 84.4 degrees at ω_c.*

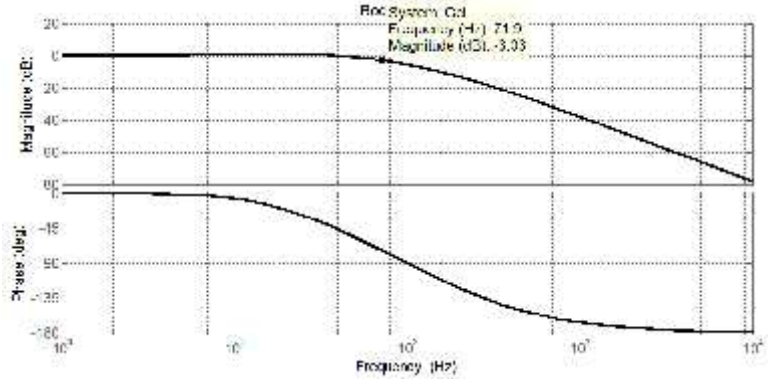


Figure 5: *Bode plot of the closed-loop system displaying the low pass characteristics.*

III. Novel Sliding Goertzel DFT (SGDFT) Algorithm for Phase Detection

Fig.6 The proposed system consists of SGDFT, Moving average filter, PI controller and Numerically Controlled Oscillator (NCO). This section describes the detailed analysis of proposed SGDFT for phase detection.

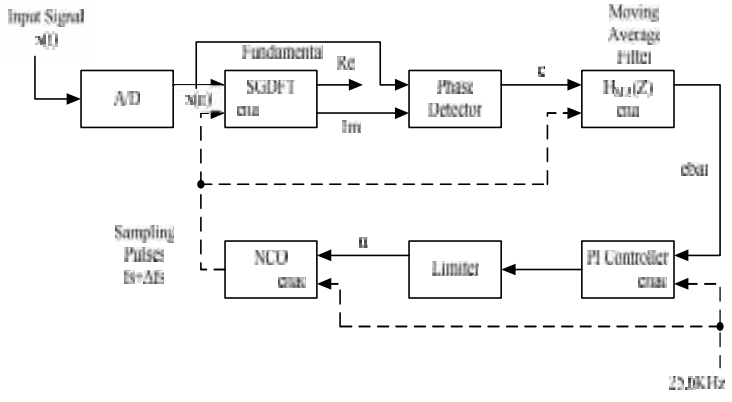


Fig.6. Block diagram of Novel SGDFT based PLL

1.1. SGDFT

In the proposed SGDFT[11], the computation involves for N samples and the SGDFT requires N+2 real multification and 3N+1 real addition, As a result, SGDFT filtering is more efficient as it requires small number of operations to extract a single frequency component [9].

Moreover, SGDFT is a versatile algorithm capable of extracting in phase and quadrature components of fundamental frequency from distorted grid voltages. In this work SGDFT filter is designed for the signal with the fundamental frequency of f, window width N, and the sampling frequency f_s. If it is driven by another signal whose frequency is f+Δf ,the sin and cosine output show a phase shift of ΔΦ which is proportional to Δf_s. This property is highly useful for phase detection, which adjusts f_s to $f_s+\Delta f_s$ making the use of ΔΦ. In addition to that, the proposed SGDFT compute the N-point for a single bin (k), cantered at an angle $\theta_k=2\pi k/N$ rad, on the unit circle, which is corresponding to the cyclic frequency of kf_s/N Hz. The bin index k is 0≤ k< N. However, for successful implementation of SGDFT, the sampling frequency f_s should be equal to the nominal fundamental signal frequency(f) and window width N. Thus the SGDFT phase detection is a real-time signal processing algorithm which is insensitive to harmonics distortion and robust against frequency and phase variations [8].

$$v(n)=2cos\left(\frac{2\pi k}{N}\right)*v(n-1)-v(n-2)+x(n)-x(n-N) \qquad (15)$$

$$y(n)=v(n)-e^{\frac{j2\pi k}{N}}v(n-1) \qquad (16)$$

Take Z transform for equation (15) and (16) and substitute equation (15) in equation (16)

The N-point SGDFT equation [12]

Where $x(n-N)$ is delay input sample and

$x(n)$ is current input sample.

The transfer function in the z-domain for the k^{th} bin SGDFT is

$$[H(Z)]=\frac{\left(1-e^{\frac{j2\pi K}{N}}Z^{-1}\right)\left(1-Z^{-N}\right)}{\left(1-2\cos(2\pi k/N)Z^{-1}+Z^{-2}\right)} \qquad (17)$$

The factor $1-Z^{-N}$ is a comb filter of the finite-impulse response (FIR). The real and imaginary component of $H(z)$ can be generated from equation (3). The structure of SGDFT for k^{th} bin is shown in Fig.7. The real and imaginary component of $H(Z)$ is given as;

$$Re[H(Z)]=\frac{\left(1-\cos(2\pi k/N)Z^{-1}\right)\left(1-Z^{-N}\right)}{\left(1-2\cos(2\pi k/N)Z^{-1}+Z^{-2}\right)} \qquad (18)$$

$$\mathrm{Im}[H(Z)]=\frac{\left(1-\sin(2\pi k/N)Z^{-1}\right)\left(1-Z^{-N}\right)}{\left(1-2\cos(2\pi k/N)Z^{-1}+Z^{-2}\right)} \qquad (19)$$

In the phase detector, the exact cosine signal obtained from fundamental SGDFT bin (k=1) is multiplied with the input signal to yield e. The output from the phase detector is given to moving average filter in order to reduce the phase margin. The output of the moving average filter is processed by a PI controller, which provides the control input for numerically controlled oscillator (NCO) with zero steady state error. Hence NCO generates the sampling pulses at required rate.

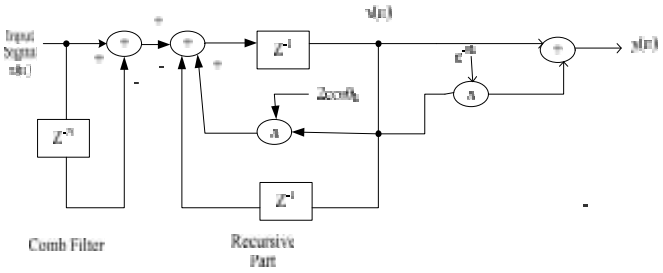


Fig..7. SGDFT structure

1.2. PI Controller

In order to provide the steady dc input ~ to the NCO, even when the phase error tends to zero at steady state, a PI controller is combined with the phase detection circuit. Thus the transfer function of the controller in the frequency domain is

$$H_{PI}(Z)=K_P+\frac{K_pT_{enao}}{T_i(1-Z^{-1})} \qquad (20)$$

where K_p is the proportional gain, T_i integral time constant and T_{eno} is the enabling time, for the PI block. The enabling frequency $f_{eno}=1/T_{eno}$ was fixed at 25.6 kHz. The output of the PI controller is limited to ±1. And the Saturation limits are allowed to prevent overflow of the integrator registers, which can incidentally limits the control input ~ applied to the NCO.

1.3. Frequency response characteristic

The frequency response characteristic of SGDFT filtering defines the noise rejection capability and phase response of the system, and can be calculated from the Z-transform of the equation (17). From that, pole-zero plot for SGDFT filtering is plotted and is given in Fig. 8. And it reveals that, two poles are cancelling with zeros and N-2 zeros equidistantly spaced on the unit circle. The extraction of single frequency component produces two poles that cancel with zeros. The poles are located on the unit circle and therefore the SGDFT filter is stable [9] [11]. The frequency characteristics of a single-bin

sliding filter for N=128 and k=1 is illustrated in Fig.9. It states that, the corresponding to the value of 'k', it allows the fundamental frequency component of grid voltage with rejection of all sub and higher order harmonic components. So it reveals neither passband nor stopband characteristics of the filter, but they adequate for coherent sampled signals [11].

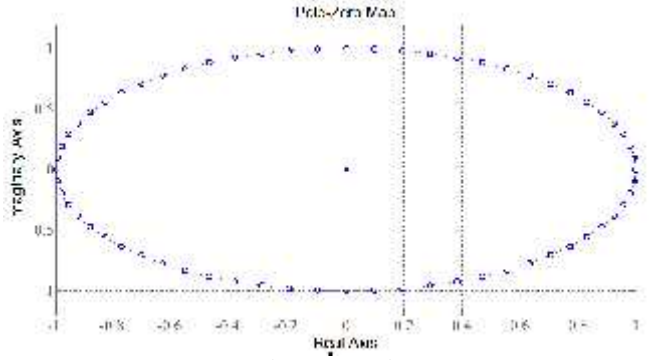


Fig..8. Pole-Zero plot for a SGDFT filter with N=128, k=1

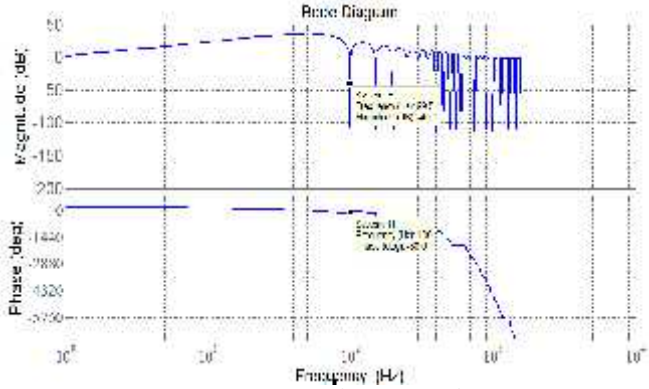


Fig.9. Frequency response of the SGDFT filter, N=128

IV RESULTS AND DISCUSSION

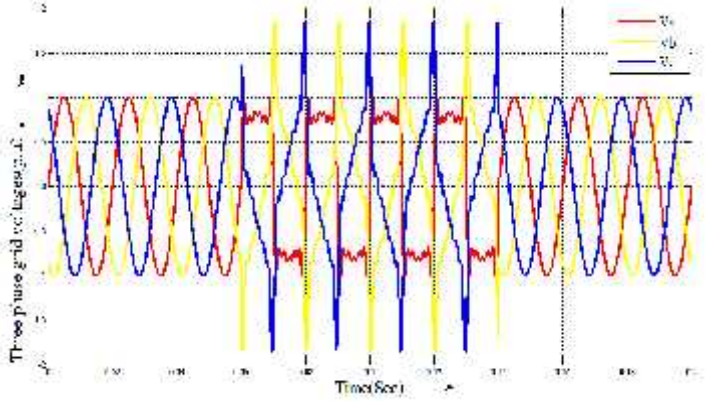
In order to analyze the proposed study simulations tests has been carried out in the MATLAB-Simulink environment and the following parameters are considered for the study. Input voltage V_m= 1 V (per unit), f=50Hz, N=128, f_{enao}=25.6 kHz, K_P=0.01 and K_I=0.0026.

The abnormal conditions namely: harmonic injection and frequency variation of grid voltages are examined for accurate phase detection using SRF PLL and SGDFT algorithm.

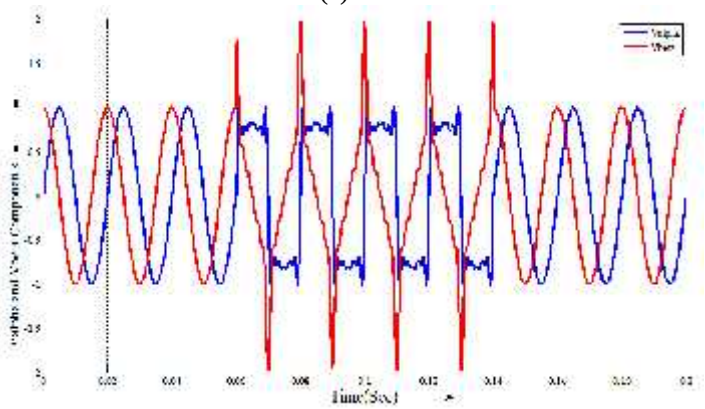
A. Response of SRF PLL

1) Harmonic Injection

The three phase input signal contains fundamental frequency of 50 Hz (1 p.u), with 33% of 3rd (0.33 p.u) , 25% of 5th (0.25 p.u) , 17% of 7th (0.17p .u) , 13% of 9th (0.13 p.u) and 8% of 11th (0.08pu) harmonics, shown in Figure.10(a). Then, V_α and $V_ß$ signals are extracted by *abc/αß* transformation and the results are shown in Figure.10(b) which is followed by αß/dq transformation and the estimated phase angle is tracked by synchronizing the voltage space vector along q-axis as shown in Figure 10(c). The true and estimated phases and estimated frequency is shown in Figure10(d) and Figure10(e), respectively. The Total Harmonic Distortion (THD) of the harmonic content in the input signal is 26.79% and fundamental signal extracted by SRF PLL (the THD of the extracted signal is 6.51%) as shown in Figure 10(f) and Figure 10(g), respectively.



(a)



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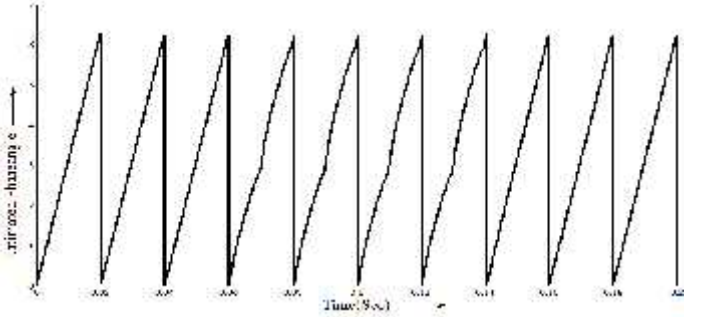

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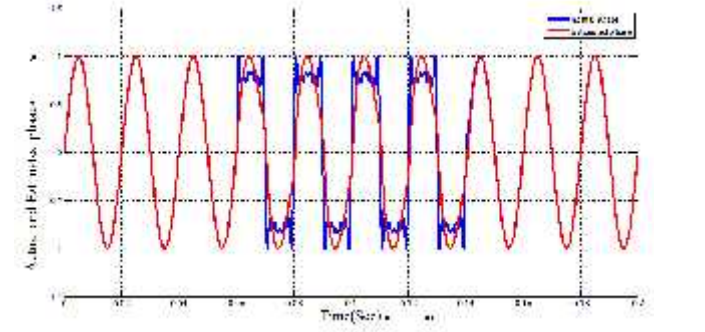
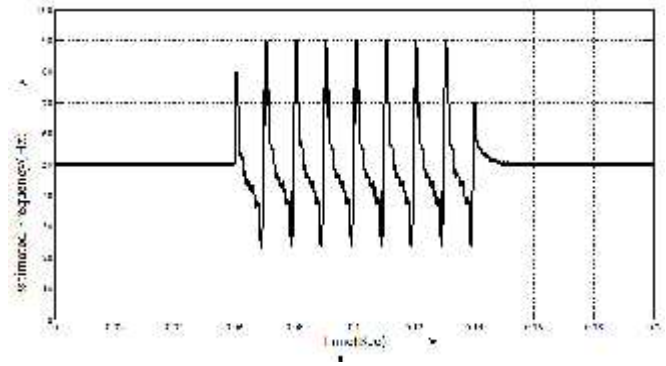


(d)



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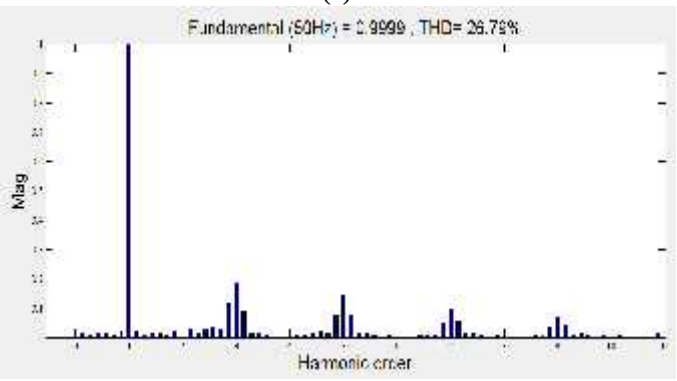

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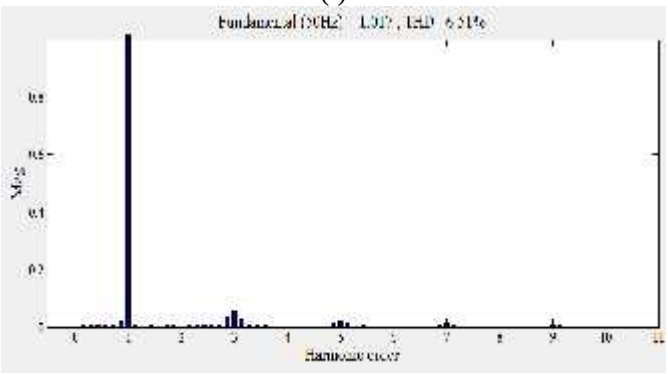

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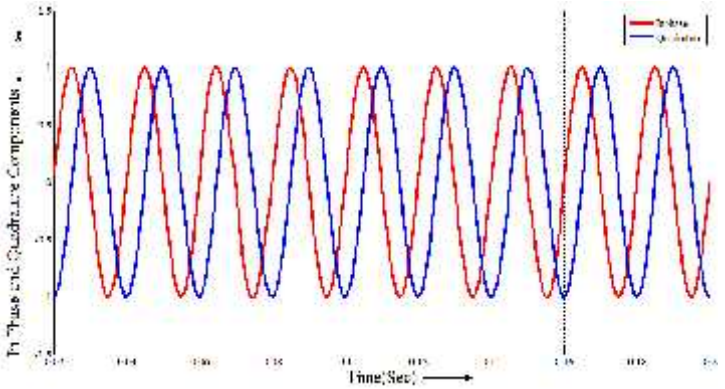
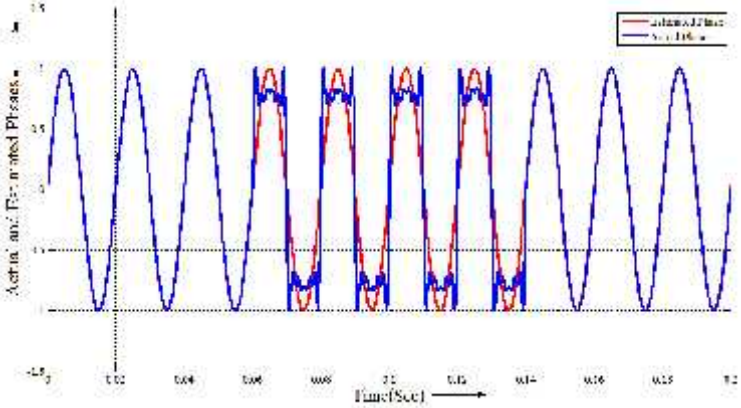


(a)



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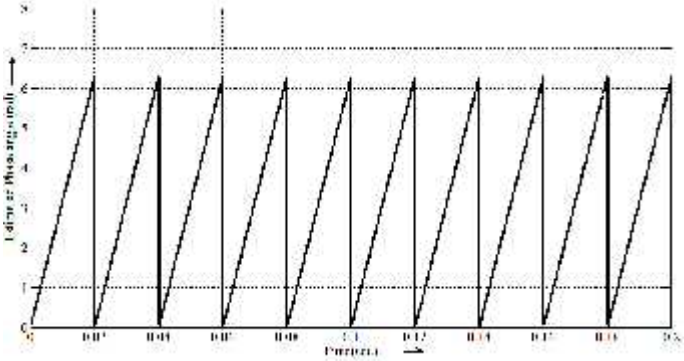

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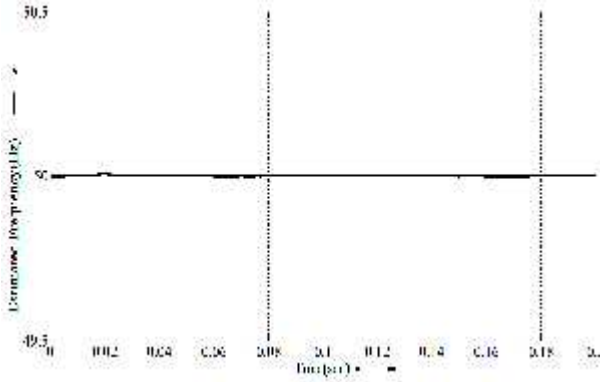


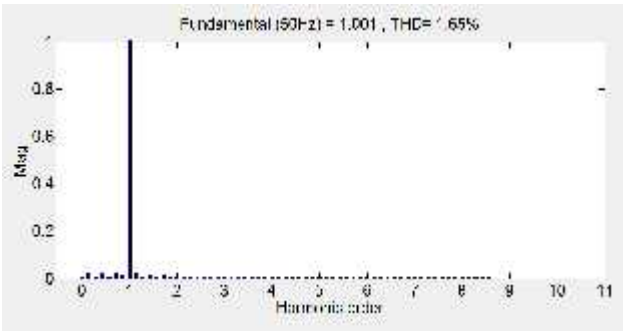
(d)

Figure 10: ***Response*** *of SRF PLL during harmonic injection. (a) Three phase input signal with harmonic injection. (b) V_α and $V_ß$ signals. (c) Estimated Phase angle. (d) Actual and Estimated Phases (e) Estimated frequency. (f) Harmonic content Input THD.(g)Estimated Output THD.*

B. Response of DFT Algorithm

Harmonic Injection

By injecting the same harmonic content three phase input signal as shown in Fig.10 (a) to DFT filtering algorithm, the fundamental frequency component is accurately extracted as compared to SRF PLL.The corresponding estimated Inphase and quadrature signals are shown in Fig.11 (a). The actual and estimated phases, estimated phase angle and estimated frequency are extracted at accurate sampling rate by using NCO as shown in Fig.11(b), Fig.11(c) and Fig.11(d) respectively. As a result, the THD of grid voltage is reduced to 1.65%. as shown in Fig.11 (e).



(e)

Figure 11: *Response of SGDFT filtering during Harmonic Injection. (a) Inphase and quadrature components. (b) Actual and Estimated phases. (c) Estimated Phase angle. (d) Estimated frequency (e) Estimated output THD.*

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TABLE I- COMPARATIVE ANALYSIS BETWEEN DFT AND SLIDING DFT FILTERING

SI.No	Parameters	SRF PLL	SGDFT PLL
1	THD of grid voltages	6.51%	1.65%
2	Fundamental component extraction	Less Accurate	Accurate
3	Stability	unstable	stable
4	Steady-state error in frequency tracking	large	Small

IV. CONCLUSIONS

This work proposes and alternative method of phase detection based on SGDFT algorithm for grid synchronization of distributed grid condition. From the proposed study it was observed that, SGDFT phase detection system is more efficient as it requires small number of operations to extract a single frequency component, thereby reducing computational complexity. Moreover, the transient response of the proposed recursive DFT is very fast as compared to conventional SRF PLL with lower THD of grid voltages/currents. The proposed synchronization scheme that in addition to detecting the grid phase angle can detect current harmonics and extract the active/reactive current component for power quality purposes. Thus the proposed phase detection system that in addition to detecting the grid phase angle and frequency can detect voltage harmonics and extract the active/reactive voltage component for power quality purposes. Therefore, the immediate advantages of the proposed PLL are: frequency adaptability, high degree of immunity to disturbances and harmonics, and structural robustness. Moreover, the proposed synchronization scheme can further be used for grid measuring, monitoring and processing of the grid signal.

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