A LabVIEW Based Condition Monitoring System for Cascaded H-bridge Multilevel Inverter

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***Abstract*—Multilevel inverters (MLIs) have wide range of applications in industry; however, the increased number of components in MLIs, increases probability of fault drastically. In order to ensure reliable operation a proper condition monitoring system is required. Such a condition monitoring system ensures protection, fault prediction, fault detection and diagnosis (FDD), and fault tolerant operation. This paper, presents a LabVIEW based condition monitoring system for a cascaded H-bridge (CHB) MLIs. As the LabVIEW has all provisions for acquiring and interfacing with a hardware setup, this makes a practically simple and powerful monitoring platform.**

Keywords—Cascaded H-bridge (CHB), condition monitoring, fault detection, fault diagnosis, multilevel inverter (MLI), , open-transistor fault

I. INTRODUCTION

MLIs are getting a lot of attention for DC-AC power conversion due to many advantages like capability to operate higher voltages using traditional semiconductors, reduced common mode voltages, reduced dv/dt stresses and staircase waveforms with better harmonic profile [1]. They are used in many industrial applications such as in industrial applications such as compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro-pumped storage, wind energy conversion and railway traction etc. [2-3]. The classical multilevel inverter topologies are neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) and different topologies are also available with decreased number of components and reduced complexity, a lot of researches are going on this area [1, 4-5].

An MLI topology consists of number of DC sources, power electronics devices, capacitors etc. As number of components increases probability of fault will also increase. It may be difficult to check each component manually whenever there is a fault, so an effective condition monitoring system has to be incorporated along with the control of the MLI-fed application. Such a condition monitoring system ensures protection, fault prediction, fault isolation, fault detection and diagnosis (FDD) and fault tolerant-operation [6]. This paper, presents a LabVIEW based condition monitoring system for MLIs. As the LabVIEW has all provisions for acquiring and interfacing with a hardware setup and real-time data and signal analysis, this makes a practically simple and powerful monitoring platform with ease of use.

In this paper, a condition monitoring system for CHB-MLI has been realized and configured for open-transistor fault detection and diagnosis. In this method, the output voltage has been used as the diagnostic variable for the FDD [7]. Intelligence based methods such as Fast Fourier Transform and neural networks, voltage histogram and neural network and particle swarm and neural network can also be implemented in LabVIEW [8-10].

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded-H bridge multilevel inverter consists of series connected H-bridges with isolated DC sources. The output voltage of inverter is the sum of each H-bridge voltage. A CHB-MLI topology with two H-bridges is shown in Fig. 1. There two configurations are possible with CHB-MLIs. In the symmetrical configuration in which DC sources is of equal value and asymmetrical configuration with different value of DC source. The relation between output voltage level (N) and number of bridges (H) for symmetric and asymmetric CHB-MLIS are given as follows,

Symmetric configuration:

$$N = 2H + 1;\ V_{dcn} = V_{dc} \quad for \quad n = 1, 2, ...H \tag{1}$$

Asymmetric configuration:

$$N = 2^{(H+1)} - 1; V_{dcn} = 2^{(n-1)} V_{dc}\ ;\ for\ n = 1, 2, ...H \tag{2}$$

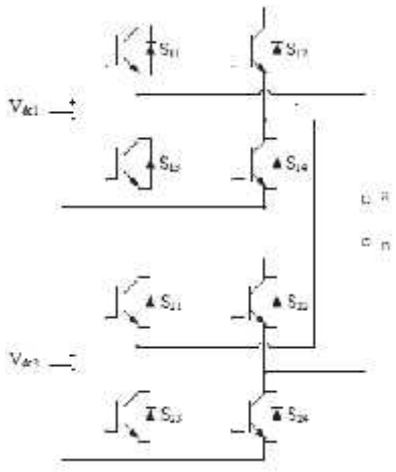


Fig. 1. Cascaded multilevel inverter topology.

By using the asymmetric configuration, it is possible to attain higher number of levels by using asymmetric configuration without increasing the component count. The topology shown in Fig. 1 can achieve output levels of 'five' in symmetric mode and 'seven' in asymmetric mode. In this paper, the asymmetric configuration of CHB-MLI is investigated. A 7-level (asymmetric) CHB-MLI involves comparison of six carriers and one sinusoidal reference signal. The PWM pulses are generated by the comparison of the sinusoidal reference signal of 50Hz with phase disposed triangular carriers of 1 kHz frequency with a modulation index of 0.8 and the switching table used asymmetric (7-level) configurations is given in Table I.

TABLE I. SWITCHING TABLE OF ASYMETRIC CHB-MLI

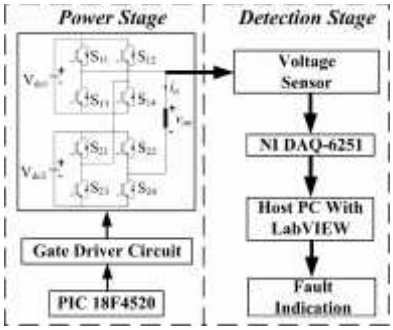
Output Voltage	**Switching States** (1=On, 0=Off) **Asymmetric** (V_{dc1}=40V, V_{dc2}=80V)							
	S_{11}	**S_{12}**	**S_{13}**	**S_{14}**	**S_{21}**	**S_{22}**	**S_{23}**	**S_{24}**
$V_{dc1}+V_{dc2}$	1	0	0	1	1	0	0	1
V_{dc2}	1	1	0	0	1	0	0	1
V_{dc1}	1	0	0	1	1	1	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc1}$	0	1	1	0	1	1	0	0
$-V_{dc2}$	1	1	0	0	0	1	1	0
$-(V_{dc1}+V_{dc2})$	0	1	1	0	0	1	1	0

III. LabVIEW BASED CONDITION MONITORING SYSTEM

The basic task of condition monitoring starts with sensing of system parameters such as current, voltage, speed, torque, etc. These signals consist of information about the system under normal and fault conditions. For the better understanding of operating conditions of the system, feature such as mean value, Fast Fourier Transform (FFT), total harmonic distortion (THD) etc. are extracted from the sensed signal. Then, features are analyzed by means of signal-model or process model based methods such as limit checking, trend checking, correlation, spectrum analysis, parameter estimation, state observers etc. and by comparing to their nominal values malfunction or fault can be detected. Once the presence of fault is detected, the next step is diagnosis of fault, involving determine type, size, location and cause of the fault. Depending upon the hazardous class of the fault, the fault detection algorithm decides the further step to be done, whether a fail-safe state, reconfiguration, fault tolerant operation or shut down for maintenance or repair.

In this paper, a condition monitoring system based on LabVIEW, for CHB-MLI is proposed. A prototype of a CHB-MLI having two H-bridges (*H*=2) with gate driver circuit and RL-load has been implemented, which is used for experimental verification. The DC source voltages are selected as V_{dc1}= 30V and V_{dc2}=60V, so that a maximum output peak of 90V cam be achieved. The FGA15N120 IGBTs with internal anti-parallel diodes are used for the prototype. The modulation scheme is implemented using PIC18F4520. The proposed setup senses the output voltage (v_{ao}) using calibrated voltage (LEM® LV-25p) sensor to host-PC through a data acquisition card (NI®-6251) [11]. The host is installed with LabVIEW software [12]. The block diagram and the experimental setup are shown in Fig. 2.

This condition monitoring system has been configured to detect and diagnose the open-transistor fault in CHB-MLI. The FDD method presented in [7] is adopted in this work. In which the mean value of the output voltage has been used as the diagnostic variable. Based on the mean values under healthy and fault conditions the open-transistor fault can be detected and faulty switch can be identified. This algorithm has been implemented in LabVIEW using pallets and the snapshot of the LabVIEW algorithm is shown in Fig. 3.



(a)

(b)

Fig. 2. (a) Block diagram (b) experimental setup of condition monitoring system.

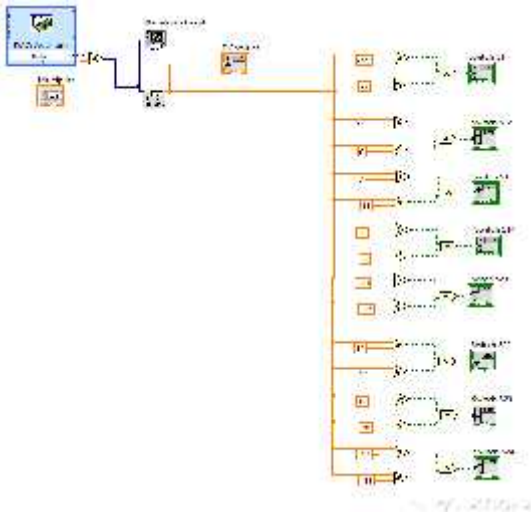


Fig. 3. FDD algorithm implementation in LabVIEW.

IV. RESULTS AND DISCUSSION

The output voltage waveform of the asymmetric CHB-MLI (7-evel) under normal operating condition is shown in Fig. 4. In this paper, open transistor fault on one switch is considered at a time, as fault in more than one switch is very rare. Now, the open transistor fault is introduced to a properly working MLI, by removing the gate pulse from the corresponding switch. In effect, it results in the open transistor fault condition. In this case the fault has been introduced to Switch 'S12' (second switch of first h-bridge) and the corresponding output voltage waveform is shown in Fig. 5. It can be inferred that fault results in change in output voltage waveform result in introduction of mean value in the output voltage. Based on this the fault can be detected and based on the mean value and its polarity faulty switch can be identified. Table II indicates the mean value corresponding to normal conduction and corresponding fault switches.

At every instant, the voltage current signals are sensed and analyzed by the FDD strategy implemented in LabVIEW. Whenever a fault occurs, it results in change in mean value of the output voltage. Based on this the FDD algorithm detect the fault and identifies the faulty switch. Further, a real time indication is also generated in a user-friendly was to infer the faulty switch as shown in Fig. 6.

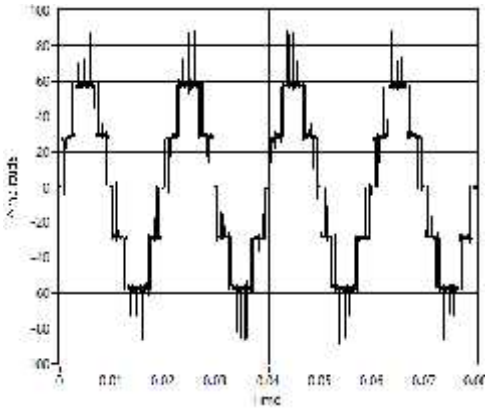


Fig. 4. Output voltage waveform under normal operating condition.

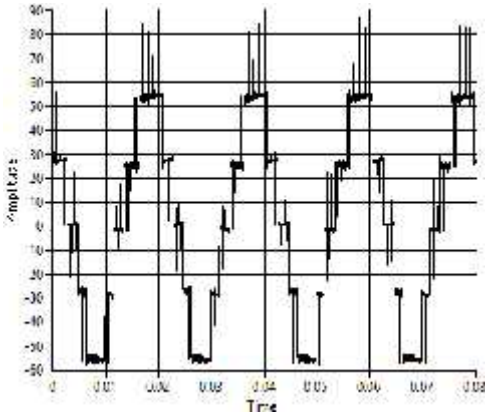


Fig. 5. Output voltage waveform under switch 'S12' under open-transistor fault condition.

TABLE II. OUTPUT VOLTAGE FEATURES OF 7-LEVEL ASYMETRIC MULTILEVEL INVERTER UNDER FAULTY CONDITIONS

Faulty Condition	Mean Value (V)
Healthy	0
S_{11}	-17.8
S_{12}	9.603
S_{13}	17.8
S_{14}	-9.603
S_{21}	-30.26
S_{22}	25.23
S_{23}	30.26
S_{24}	-25.23

Fig. 6. Fault indication for fault in switch 'S12'.

V. CONCLUSION

Multilevel inverters have wide range of application, but increased number of components increases probability of fault. Therefore, an efficient condition monitoring ensures protection and reliable operation. In this paper, a condition monitoring system for CHB-MLI based on LabVIEW is discussed. This condition monitoring system has been used to realize a fault detection and diagnosis strategy for open-transistor fault in CHB-MLIs. The proposed, scheme is experimentally verified and the results prove that the proposed FDD strategy detects and identifies the faulty switch instantaneously.

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