Hybrid PWM switching scheme for a three level neutral point clamped inverter

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Abstract- The motivation of this project was to design a hybrid switching scheme for a three level neutral point clamped inverter. The three-level inverter helps to reduce the total inverter losses at higher switching frequencies, compared to a two-level inverter. The three-level inverter has also more power switches compared to the two-level inverter. This helps to reduce the voltage stress across the switches and the machine winding. In addition, it also allows an increase in the DC-link voltage, which in turn helps to reduce the DC-link current, phase conductor size and the associated losses. Moreover, at higher DC-bus voltages the power switches will have lower thermal stress when compared to the 2-level. However, the NPC inverter topologies have an inherent problem of DC-link voltage balancing. Here in this paper, a novel switching scheme for a three level NPC inverter with neutral point voltage balancing algorithm has been designed. The switching scheme is a hybrid one, which incorporates the advantages of both carrier based and space vector based PWM switching schemes.

I. INTRODUCTION

Multilevel inverters are increasingly being used for lowpower, medium-power, and high-power applications, due to significantly lower harmonic distortion and lower voltage stress across the switches [1]. Compared to 2-level inverters, 3-level inverters depict superior voltage and current harmonic spectrums, lower switching losses at higher switching frequencies, and lower source-side EMI issues [2], [3]. However, 3-level neutral-point-clamped (NPC) inverters depict a potential problem of DC-link capacitor voltage unbalancing. There are other additional advantages like a reduction in total harmonic distortion (THD) due to an increase in the number of voltage steps, which then reduces EMI emission and high dv/dt stress across semiconductor switches. Other typical problems associated with two-level inverters like stator winding insulation break down and bearing failures can also be significantly reduced in three-level inverters. Multilevel inverters can be divided into three categories, such as H-Bridge Inverter, Flying Capacitor Inverter, and N-Level Neutral-Point-Clamped (NPC) Inverter.

Various modulation schemes have been developed for 3- level inverters, with neutral point voltage balancing scheme. They can be classified into three categories namely, Selective Harmonic Elimination (SHE), Carrier-Based PWM (CBPWM) and Space-Vector Pulse-Width Modulation (SV- PWM). Among these options, CB-PWM is the simplest to implement. It directly generates the duty cycles for the switches from the reference-voltage vector, instead of sector identification and extensive numeric calculations for the switching periods, as in case of the classical SV-PWM strategy.

In [4] a carrier-based DC-link voltage balancing strategy based on neutral point current is derived. Although, results show desired steady-state performance, the proposed system is complicated for hardware implementation, since it requires intense mathematical computation. A reduced switching loss based Carrier-PWM strategy is proposed in [5]. In this strategy, one of the phases is clamped to the positive, negative, or neutral point of the inverter, depending on the two capacitor voltages. Though experimental results show a reduction in the capacitor voltage difference, detailed transient performance is not carried out. A double carrier based DC-link voltage

balancing strategy is shown in [6]. An optimum value of DC-offset value is also analytically derived. However, results show a lot of neutral point voltage ripple and no transients results are shown to verify the efficacy of the system with transient load variations.

In [7], [8] a nearest-three-vector (NTV) scheme is shown which uses the redundant voltage vectors to keep the capacitor voltages balanced based on the redundant voltage sharing factor. However, the numbers of switching sequences in different subsectors are different, which leads to asymmetrical switching. To make the switching sequence symmetrical in each subsector, the subsectors 1-2 are further subdivided into two regions. It makes the switching sequence symmetrical; however it increases the system complexity. Moreover, symmetrical switching schemes have more low frequency voltage ripple than the conventional NTV schemes. In [9] another voltage balancing strategy based on redistribution of the redundant vector states is proposed.

All proposed carrier and NTV based strategies uses the DC-offset or use the redistribution of the redundant voltage vectors to keep the neutral point potential (NPP) balanced. However in transients the DC-offset or value of redundant voltage sharing factor can go out of limit and disturb the NPP. To overcome this problem a symmetrical lower switching loss based DC-link voltage balancing strategy is proposed in [10]. It uses only five vectors in each switching cycle, which reduces the switching losses compared to the conventional NTV schemes, and also keeps the two capacitor voltages balanced even at rapid speed and torque variations. However, the SVPWM based strategies are computationally intensive, due to the presence of numerous mathematical calculation of sector identification, and duty ratio calculation for each vector.

PWM based control strategies for 3-level inverters can be divided into three categories [60]: 1. Selective-harmonic-elimination (SHE), 2. Carrier-based PWM (CB-PWM), and 3. Space vector PWM (SV-PWM).

Selective-Harmonic-Elimination (SHE) Based PWM Strategy:

Selective harmonic elimination strategy provides certain advantages over other PWM based control strategies [61]-[64]; such as reducing the switching losses by reduced switching, better utilization of the DC-link voltage and higher power quality by reducing the lower order harmonic components. However, all the SHE strategies proposed so far are based on the generation of commutation angles. These angles are generated by equating the equation of the harmonic components to zero, that are required to eliminate. Solutions of these equations are computationally cumbersome and take a lot of processor memory and processing time. Hence, most of the SHE strategies are generally used for high and medium power applications, where switching frequencies are in the range of 200-800 Hz and power frequency of 0-50 Hz. Moreover, no DC-link voltage balancing strategy is shown with the SHE strategy, which will make the system more complicated for multilevel inverters. The DC-link of these inverters is generally supplied by separate three-phase rectifiers across each capacitor for NPC inverters. Hence, for electric vehicle applications where, machine speed goes as high as 800.0 Hz and the DC-link balancing strategy will also be incorporated with the PWM strategy, SHE technique could not be of great interest.

Carrier PWM Based Strategy:

Based on the SPWM control strategy, a switching frequency optimized PWM control (SFO-PWM) was introduced for NPC inverters, with DC-link voltage balancing [65]. In this strategy, depending on the DC-link capacitor voltage deviation, offsets were used in addition to the reference three-phase voltage signals. Because of SPWM, this strategy is not easily able to utilize DC-link capacitor voltage efficiency, compared to SV-PWM strategy. Large values of DC-link capacitors are used, which helps reduce the DC-link capacitor voltage deviation. On the other hand, the proposed strategy has not been tested for a wide range of speed and torque variation, to show performance efficiency.

A hysteresis controller for capacitor voltage balancing is presented, which keeps the two DC-link capacitor voltages within a certain tolerance band. Unfortunately, this technique has no restriction on the choice of switching state, and simultaneous switching may occur. Instantaneously switching an output through more than one level can result in significant voltage stressing of devices. Also, test results show that the neutral point rapidly diverges, when the control signal is removed. However, without sharing the redundant states, the PWM controller itself

becomes unbalanced, and neutral point divergence is unavoidable.

Another DC-link voltage balancing scheme is also proposed based on integration of neutral point capacitor current. In this study, the effect of a regenerative condition on capacitor balancing is also considered. An improved carrier based PWM (CB-PWM) is also proposed based on NTV-SVM strategy. In this strategy, a zero-sequence component of voltage, based on capacitor voltage unbalance, is added to the reference voltage signal. Performance comparison with SPWM strategy, based on NP voltage oscillation, is also studied. However, applications of the proposed system with system transients are not shown. Moreover, addition of zero-sequence voltage components with the reference voltages could lead to a modulation value, which can clamp one of the phase voltages. This situation can create further unbalance at the neutral point.

A carrier-based PWM strategy is introduced, which is capable of eliminating low order harmonics. However, it increases the switching frequency by one-third compared to conventional SV-PWM techniques. In this control strategy, DC-link voltage deviation is reduced by shifting the modified modulation signals in accordance with the capacitor voltage differences. However, no transient results are shown to demonstrate the DC-link voltage balancing ability of the scheme and the system takes a considerable time before converging. A PI controller is proposed to calculate the NPP fluctuation with a carrier based PWM technique. In this strategy, neutral point current is integrated for one switching cycle, and then it is subtracts from zero, and passes through a PI controller, to generate the duty for redundant voltage vectors. Although experimental results show that the proposed control strategy is capable of keeping the neutral point voltage stable, the system is highly dependent on the PI gain.

As the SVPWM and carrier based strategies are symmetrical a hybrid PWM strategy is proposed in this paper. It uses both the advantages of carrier based strategy and SVPWM strategy to generate the duties for the power switches and keep the DC-link capacitor voltages balanced even at torque-speed transients, such as those in electric vehicle (EV) application. The proposed hybrid PWM strategy uses the carrier based strategy to generate the duty cycle of the power switches, which does not take into account the NPP stability. Once the gating signals are generated the redundant vectors are used to keep the NPP balanced.

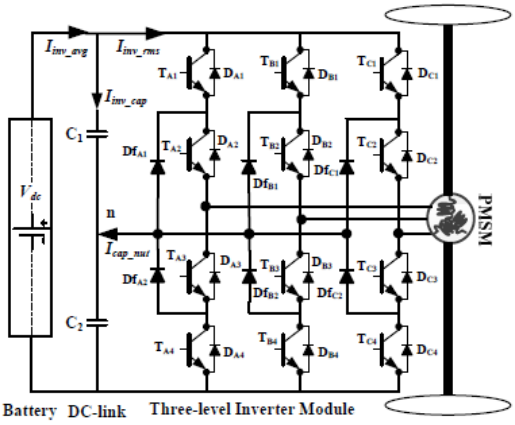

Figure 1 Three-level neutral point clamped (NPC) inverter for EV traction.

II. PRINCIPLE OF OPERATION

A. Space-Vector PWM (SV-PWM) for 3-Level Inverter

As can be seen from the 3-level NPC inverter (Fig. 1), the inverter has 4 switches for each leg. There exist 2 diodes in each leg, whose neutral point is connected to the common connection point of the two DC-link capacitors. Hence, there exist a total of 27 switching combinations, out of which 3 are null or zero-vectors, and 24 are active vectors, as shown in the phasor diagram of Fig. 2. Table I shows the different switching combinations and output pole voltages. Detailed calculated time periods for difference switches depending on subsectors are shown in [11].

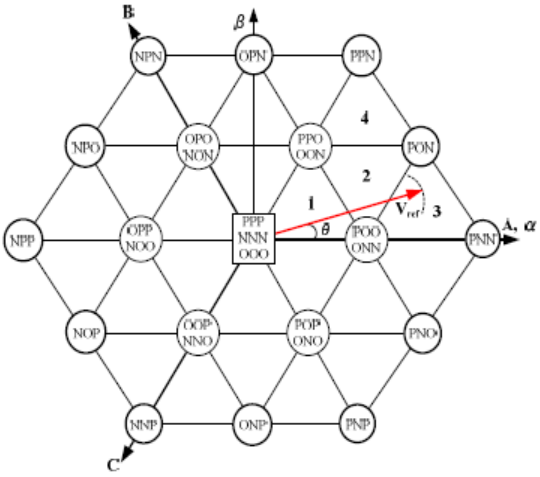

Figure 2 Space-vector diagram for 3-level NPC inverter.

Table 1 Different switching combinations.

Switching vector combination	Voltage level
PPP,NNN,OOO	0 (Null)
PPO,OON,POO,ONN,POP,ONO,OOP, NNO,OPP,NOO,OPO,NON	$V_{dc}/3$ (Small)
PON,OPN,NPO,NOP,ONP,PNO	$V_{dc}/\sqrt{3}$ (Medium)
PNN,PPN,NPN,NPP,NNP,PNP	$2V_{dc}/3$ (Large)

A generalized, fast SVM algorithm for multilevel inverters is proposed for *n* number of levels, to reduce implementation complexity. A control strategy based on small voltage vector redundancy is presented and experimentally verified. In this topology, a redundancy factor "*α*" is introduced to utilize the positive and negative small voltage vectors, which produce the same output voltage, but affects the two capacitor voltages differently. However, to compute the value of "*α*" online, it produces 1.0 m-sec of computation delay time. This is an iterative process which may introduce higher capacitor voltage deviation for application like motor drives with high load transients. Experimental results are shown only at steady state and it shows large computational delay time to reduce capacitor voltage deviation. DC-link voltage balancing for over modulation regions are also studied and implemented by researches in [90]. In this strategy conventional nearest three vector (N3V) scheme is used at modulation indices below 1 and above that the proposed strategy is used. Based on the distribution of redundant small voltage vectors, another control strategy is introduced in [91], [92]. In this topology, 4 sub-sectors are further divided in to 6, to make the number of switching sequences symmetrical.

Based on the two capacitor voltage deviation, calculated from individual capacitor currents, a capacitor voltage balancing algorithm is also proposed. Switching sequences are generally altered depending on the instantaneous states of capacitor voltages. As capacitor voltages are calculated by integration, additional computation delay time is introduced in the system. Moreover, in this strategy, both the positive and negative redundant states are used in the same switching sequence, which may influence the capacitor voltage deviation in transients.

A virtual space-vector scheme (VSVS) – an advanced PWM scheme – capable of controlling the neutral point voltage over entire range of output voltage is presented. According to this topology, the virtual point, based on the small and medium voltage vectors, is added in each sector, which helps to keep the capacitor voltage deviation at a predetermined level. However, the inclusion of an additional vector, which keeps neutral point current zero, creates a more complicated system in terms of real-time implementation and increases the switching frequency. Moreover, experimental results show only steady-state results, without any transients and rapid load variations.

B. Single- Carrier based Hybrid-PWM Control with DC-Link Voltage Balancing

The proposed control circuit for the 3rd harmonic PWM based hybrid DC-link capacitor voltage balancing is shown in the Fig. 3. The 3-phase currents and machine speed are used to generate the 3 reference phase voltages (v_{abc}). A zero-sequence voltage, v_z is then generated from the v_{abc}, as shown in eq. (1). This is then subtracted from v_{abc}, to generate the reference phase voltage (v_{abc_ref}), which is equivalent to the classical space-vector pulse-width modulation (SV-PWM) scheme. It is then converted to an appropriate duty-ratio as shown in eq. (2).

$$\begin{aligned} \upsilon_{a\_ref} &= \upsilon_a + \upsilon_o \\ \upsilon_{b\_ref} &= \upsilon_b + \upsilon_o \\ \upsilon_{c\_ref} &= \upsilon_c + \upsilon_o \end{aligned} \tag{1}$$

$$\begin{aligned} \delta_{a\_ref} &= (\upsilon_{a\_ref} / (0.5 \cdot \upsilon_{dc})) \\ \delta_{b\_ref} &= (\upsilon_{b\_ref} / (0.5 \cdot \upsilon_{dc})) \\ \delta_{c\_ref} &= (\upsilon_{c\_ref} / (0.5 \cdot \upsilon_{dc})) \end{aligned} \tag{2}$$

$$\begin{aligned} \delta_{ap} &= \delta_{a\_ref}, && \text{When, } \delta_{a\_ref} \rangle 0 \\ &= 0, && \text{When, } \delta_{a\_ref} \langle = 0 \\ \delta_{an} &= \delta_{a\_ref} + 1, && \text{When, } \delta_{a\_ref} \langle 0 \\ &= 1, && \text{When, } \delta_{a\_ref} \rangle = 0 \end{aligned} \tag{3}$$

However, the generated duty from this expression has both the positive and negative polarity. Hence, to convert the bipolar duty-ratio to unipolar format, so

that only one carrier wave can be used, a modified control strategy is derived in eq. (3). In this strategy, the negative polarity is phase-shifted by adding the negative part with unity.

The duty cycle generated in eq. (3) does not take into consideration the DC-link capacitor voltage imbalanced condition, which is a potential problem with NPC inverters. Most of the proposed control strategies use neutral point current as an indicator of voltage imbalance, which is in turn integrated to generate the DC-offset voltage. This DC-offset voltage is then added to the original duty-cycle, to generate the compensated duty. However, larger variations in the DC-offset voltage can distort the duty-cycle, and significantly affect the phase-voltage harmonics. This situation may even over-stress the inverter switches. This may lead to over-voltage breakdown of the switches, as shown in [11]. Hence, in order to generate smaller voltage harmonics, as well as reduce the voltage stress across the inverter switches, and eliminate additional PI controller requirement to generate the DC offset voltage, a hybrid-PWM strategy is proposed in this paper.

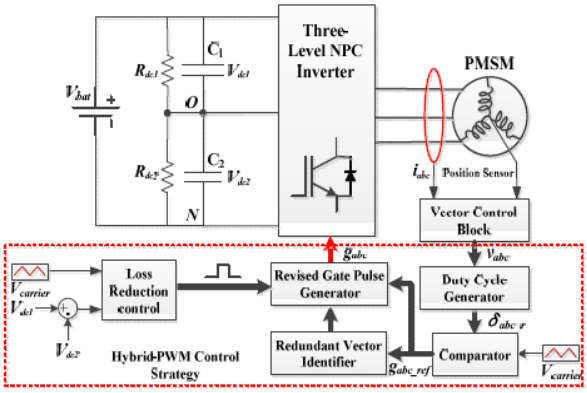

Figure 3 Block diagram of the proposed single-carrier based PWM control strategy

In the proposed hybrid carrier-based PWM control strategy, 3 logical control blocks are introduced. The loss reduction block updates the variation in the 2 capacitor voltages at the start of each switching cycle. This helps reduce the switching losses, because it restricts the change in duty cycle between each carrier frequency cycle. The output from the comparator block generates the inverter gating signals, after comparing the three phase duties with the single carrier wave. Since this block does not take care of the DC-link capacitor voltage imbalance condition, it is passed on to revised gate-pulse generator block. Another part of gate signal goes to the redundant vector identifier block, which gives information about the redundant states. If g_{abc_ref} consists any of the redundant states as shown in Fig. 3, then depending on the output from the loss reduction block, modified control pulses are generated for the inverter, as shown in Table II.

Table 2 Hybrid-PWM based DC-link voltage balancing scheme.

Redundant States	Balancing Ability	Switching state
POO	$v_{dc1} > v_{dc2}$	POO
	$v_{dc2} > v_{dc1}$	ONN
ONN	$v_{dc1} > v_{dc2}$	POO
	$v_{dc2} > v_{dc1}$	ONN
PPO	$v_{dc1} > v_{dc2}$	PPO
	$v_{dc2} > v_{dc1}$	OON
OON	$v_{dc1} > v_{dc2}$	PPO
	$v_{dc2} > v_{dc1}$	OON
OPO	$v_{dc1} > v_{dc2}$	OPO
	$v_{dc2} > v_{dc1}$	NON
NON	$v_{dc1} > v_{dc2}$	OPO
	$v_{dc2} > v_{dc1}$	NON
OPP	$v_{dc1} > v_{dc2}$	OPP
	$v_{dc2} > v_{dc1}$	NOO
NOO	$v_{dc1} > v_{dc2}$	OPP
	$v_{dc2} > v_{dc1}$	NOO
OOP	$v_{dc1} > v_{dc2}$	OOP
	$v_{dc2} > v_{dc1}$	NNO
NNO	$v_{dc1} > v_{dc2}$	OOP
	$v_{dc2} > v_{dc1}$	NNO
POP	$v_{dc1} > v_{dc2}$	POP
	$v_{dc2} > v_{dc1}$	ONO
ONO	$v_{dc1} > v_{dc2}$	POP
	$v_{dc2} > v_{dc1}$	ONO
PON,OPN,NPO, NOP,ONP,PNO	$v_{dc1} > v_{dc2}$ or $v_{dc2} > v_{dc1}$	PON,OPN,NPO,NOP,ONP, PNO
PNN,PPN,NPN, NPP,NNP,PNP	$v_{dc1} > v_{dc2}$ or $v_{dc2} > v_{dc1}$	PNN,PPN,NPN,NPP,NNP, PNP

From Table II, it can be observed that, g_{abc} is different from g_{abc_ref}, only if redundant voltage states exist. For medium- and large-voltage vectors, gating signals do

not change their sequence, since they cannot affect capacitor voltage balancing ability. Positive voltage vectors are related to the upper capacitor voltage and negative vectors are related to the lower capacitor voltage. If $v_{dc1} > v_{dc2}$, the positive vectors are utilized, and if $v_{dc1} < v_{dc2}$, the lower capacitor voltages are used. Hence, the complicated and time consuming duty-cycle calculation process of the SV-PWM strategy is replaced by a much more efficient single carrier-based strategy. The proposed strategy keeps the harmonic voltage distortion low, while maintaining a higher DC-link voltage stability even at high torque-speed transients.

III. CONCLUSION

A simple hybrid carrier-based control strategy is developed in this paper. In this strategy, duty cycles for the switches are calculated from a single-carrier based topology, and the concept of redundant voltage vectors are used to keep the two DC-link capacitor voltages stable from SVPWM strategy. As this proposed strategy uses both the advantages from carrier and SVPWM control, it is called as hybrid-PWM strategy in this paper. Detailed simulation and experimental studies are carried out to show the performance of the proposed control strategy with higher modulation index and rated torque condition. The maximum capacitor voltage deviation in both the conditions are within the limits and comparable to the simulation results. Moreover, considerable reduction in computational complexity with the proposed hybrid carrier based topology is achieved compared to the SV-PWM based strategy.

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